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Graphene/MoS_2 Hybrid Technology for Large-Scale Two-Dimensional Electronics

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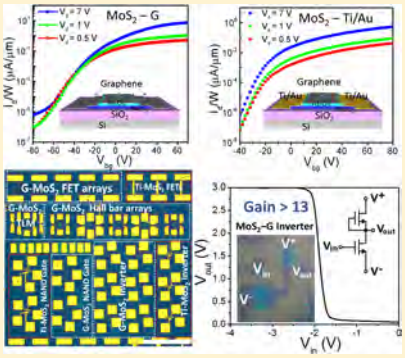
Supporting Information

ABSTRACT: Two-dimensional (2D) materials have generated great interest in the past few years as a new toolbox for electronics. This family of materials includes, among others, metallic graphene, semiconducting transition metal dichalcogenides (such as MoS_2), and insulating boron nitride. These materials and their heterostructures offer excellent mechanical flexibility, optical transparency, and favorable transport properties for realizing electronic, sensing, and optical systems on arbitrary surfaces. In this paper, we demonstrate a novel technology for constructing large-scale electronic systems based on graphene/molybdenum disulfide (MoS_2) heterostructures grown by chemical vapor deposition. We have fabricated high-performance devices and circuits based on this heterostructure, where MoS_2 is used as the transistor channel and graphene as contact electrodes and circuit interconnects. We provide a systematic comparison of the graphene/MoS_2 heterojunction contact to more traditional MoS_2-metal junctions, as well as a theoretical investigation, using density functional theory, of the origin of the Schottky barrier height. The tunability of the graphene work function with electrostatic doping significantly improves the ohmic contact to MoS_2. These high-performance large-scale devices and circuits based on this 2D heterostructure pave the way for practical flexible transparent electronics.



KEYWORDS: *Molybdenum disulfide, graphene, heterostructure, field-effect transistor, integrated circuits, flexible and transparent*

As Moore's law approaches its physical limit in Si-based electronics, the device research community has been actively searching for new material options that can push performance beyond its traditional boundaries. The emerging alternative, two-dimensional (2D) materials, offers many unique properties, making this class of materials very attractive for extending electronics into new application domains. In particular, 2D materials[1−5] with their excellent mechanical flexibility and transport properties have attracted great interest as a high-mobility alternative to organic semiconductors[6,7] and Si nanoribbons;[8] these 2D materials could lead to the realization of transparent and bendable electronic systems that can be placed on a wide variety of surfaces. To harvest their full advantage in bendable electronics, it is highly desirable to construct systems solely based on 2D materials and their heterostructures.[9−11] So far, the circuits that have been constructed based on 2D materials typically rely on a metal to form contacts and interconnects,[12−15] which is one of the key limitations on the circuit flexibility. Although there are a few reports using graphene as contacts of 2D material devices, the demonstration often remains at the level of a single device based on the nonscalable exfoliated flakes and there has been no effort reported to tune the contact performance.[10,16] Besides, a high-quality junction between semiconductor and metallic contact with no energy barrier is crucial for high-performance device, which is hard to achieve for 2D transition metal dichalcogenide (TMD) because of their large bandgap. In particular, it is essential to study the critical issues of large-scale heterogeneous integration of 2D materials and performance of graphene/2D-semiconductors. In this Letter, we address two crucial issues on future applications of 2D electronics: (i) We present the first demonstration of integrated graphene/molybdenum disulfide (MoS_2) heterostructures using a scalable chemical vapor deposition (CVD) process. Specifically,

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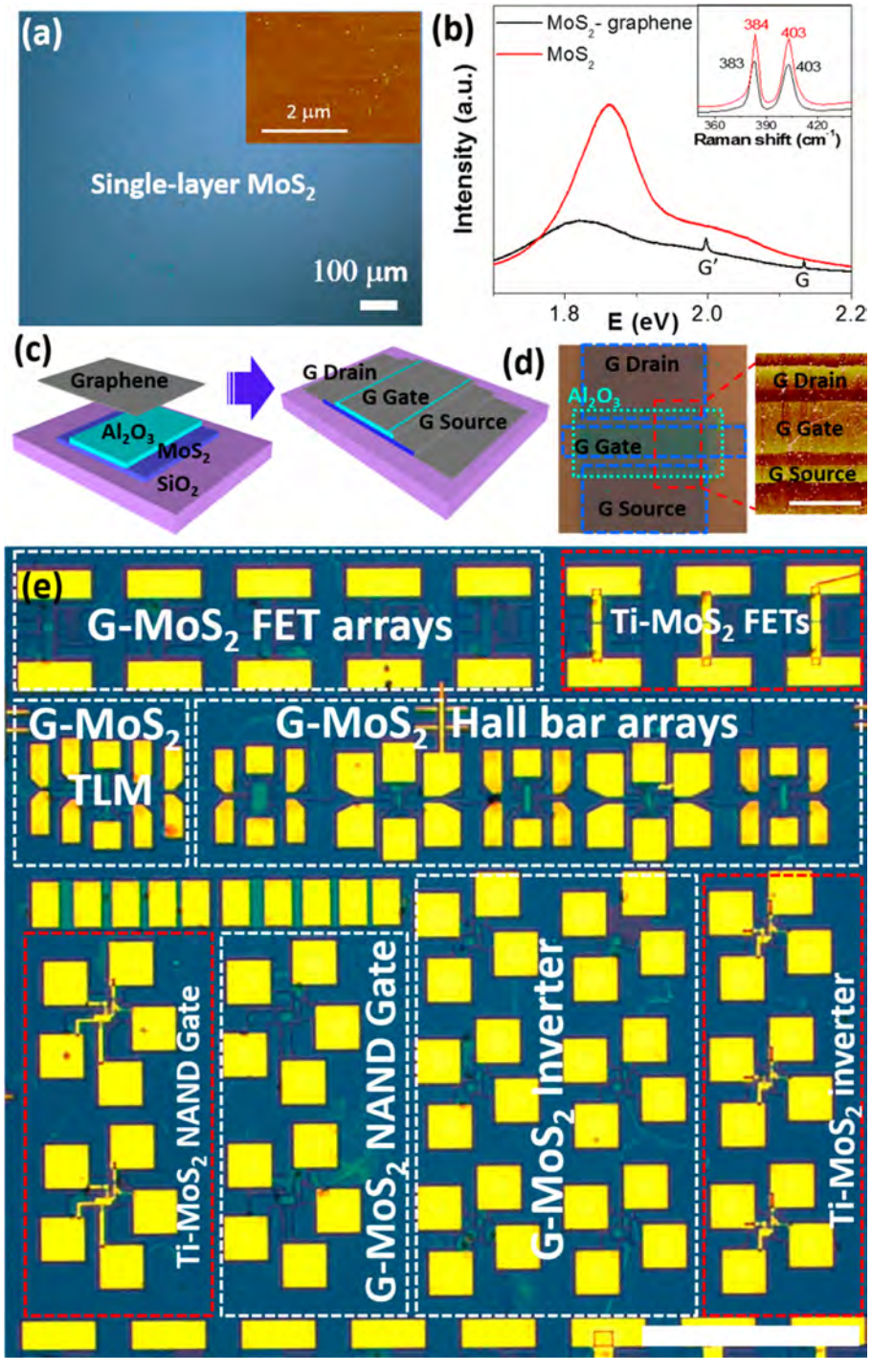

Figure 1. (a) Optical micrograph and AFM data (inset) of a single-layer (SL) chemical vapor deposition (CVD) grown MoS_2 thin film. (b) Raman spectroscopy of as-grown SL CVD MoS_2 thin film (red line) and the CVD graphene/MoS_2 structure. (c) Schematic illustration of important fabrication steps to make large-scale electronics from graphene/MoS_2 heterostructure using MoS_2 as channel and graphene as contact electrodes and interconnects. (d) Optical micrograph (left) and AFM (right) of CVD MoS_2 dual gate transistor with graphene as electrodes. The scale bar in AFM image is 10 μm. (e) Optical micrograph of large-scale chip of MoS_2 devices and circuits using CVD graphene as electrodes and interconnects (white dashed box) as well as control devices and circuits using Ti/Au electrodes in adjacent (red dashed box). Metal pads (gold color) are fabricated on the sample for convenient measurement. The scale bar is 500 μm.

we have fabricated both discrete transistors and fully integrated logic circuits using MoS_2 as the channel and graphene as contacts and interconnects by developing a new technology that allows the selective etching of 2D materials. This process can be used to fabricate any 2D heterojunction in large scale. (ii) We report on the performance of graphene-based contacts in MoS_2 field effect transistors (FETs) and systematically benchmark them against its metal counterparts. We find that the tunable Fermi level in graphene allows excellent work-function match with MoS_2, leading to low contact resistance.

Recently, high-quality TMD monolayers, including MoS_2 and WS_2, have been directly synthesized on diverse surfaces using a

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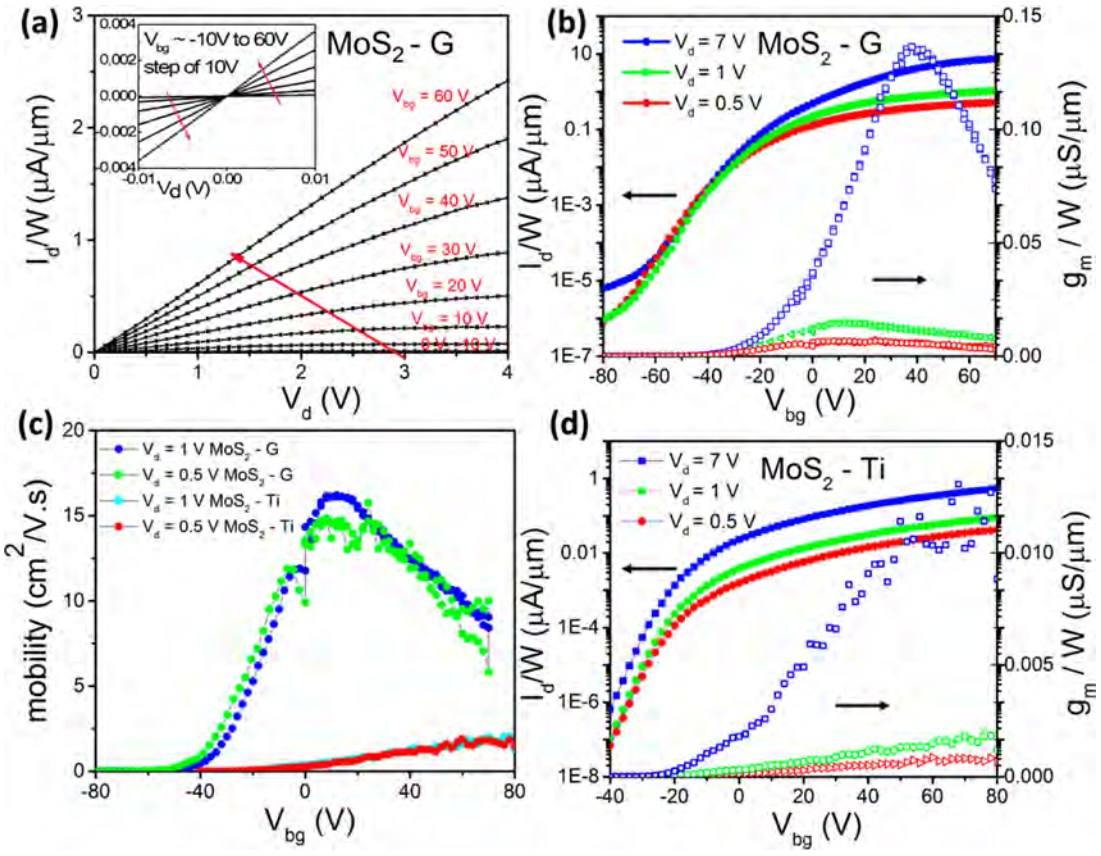

Figure 2. Back-gated transport properties of MoS_2/graphene (MoS_2−G) and MoS_2−Ti FETs performance at room temperature. (a) Output performance of a representative MoS_2−G transistor at large field and small field with both negative and positive biases (inset). (b) Transfer characteristics of MoS_2−G transistor with current density on the left axis and transconductance/width on the right axis. (c) Field effect mobilities in MoS_2−G and MoS_2−Ti FETs at different source drain voltages. (d) Same as in (b) for the control system MoS_2−Ti.

scalable CVD process with the seeding of perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS).[17,18] High-quality and large-area MoS_2 monolayers were obtained using this technique, leading to the demonstration of highly scalable electronics based on this atomically thin material.[15] We have used these MoS_2 monolayers as the channel of transistors. Details of the growth are described in the Supporting Information. An optical image of as-grown CVD MoS_2 is shown in Figure 1a, demonstrating a good uniformity and a high coverage approaching 100%. The sample is continuous over a size of 2 × 2 cm^2, ending with isolated triangular MoS_2 structures at the edge (Figure S1b, Supporting Information). Atomic force microscopy (AFM) is conducted at one of the isolated triangles to get the thickness of MoS_2 (shown in Figure S1c, Supporting Information). The thickness of the CVD MoS_2 monolayer is ∼8 Å, which is consistent with the values of MoS_2 monolayer reported elsewhere. Raman and photoluminescence (PL) spectroscopy were performed using a 532 nm Nd:YAG laser on the sample to investigate the quality of MoS_2, see Figure 1b. The single-layer structure of as-gown MoS_2 is confirmed from its Raman spectroscopy based on the peak spacing between the E_{2g} mode and the A_{1g} mode, which is smaller than 20 cm^{-1} (Figure 1b, inset). A strong photoluminescence peak located at 1.88 eV shown in Figure 1b corresponds to the carrier recombination across the direct bandgap of single-layer MoS_2[19,20] and implies a high quality of MoS_2 monolayer. Because of the large excitonic binding energy in MoS_2 (0.4−0.8 eV, from theoretic calculation),[21−23] the electronic band gap is estimated to be larger than 2.3 eV, which makes it harder to get good contact with than few layer MoS_2 (bandgap of 1.2 eV). In graphene/MoS_2 heterostructures (Figure 1b, black line), the PL intensity is quenched because the metallic nature of graphene and the PL peak shift to negative value, possibly from doping effect. The two peaks at 2.0 and 2.14 eV come from graphene Raman peak of G′ and G. There is negligible change in the peak spacing between the E_{2g} mode and the A_{1g} mode in this hybrid structure.[24]

CVD-MoS_2 monolayers grown on a 300 nm SiO_2/Si substrate were first patterned to form transistor channels using electron beam lithography (EBL) with poly(methyl methacrylate) (PMMA) as the resist. After developing the resist pattern, the exposed parts of the MoS_2 sheet are etched away using oxygen plasma to achieve device isolation. The sample was then coated with a methyl methacrylate (MMA) (6% concentration in ethyl lactate)/PMMA (2% concentration in anisole) stack, followed by EBL exposure and development, forming a double-layer structure with openings on MMA slightly wider than on PMMA. Subsequently, 20 nm aluminum oxide (Al_2O_3) was deposited by atomic layer deposition (ALD) at 100 °C (below the glass transition temperature of PMMA/MMA stack[25]) using trimethylaluminum (TMA) and water as precursors (see Methods), followed by liftoff to form a patterned Al_2O_3 etch-stop layer. Large-area single layer graphene was then grown on copper foils at 1035 °C by CVD method[26,27] and transferred[28,29] (Supporting Information) onto the sample, see Figure 1c, left panel. Following a new EBL step, patterned areas of graphene were etched by oxygen plasma to define the source, drain, and

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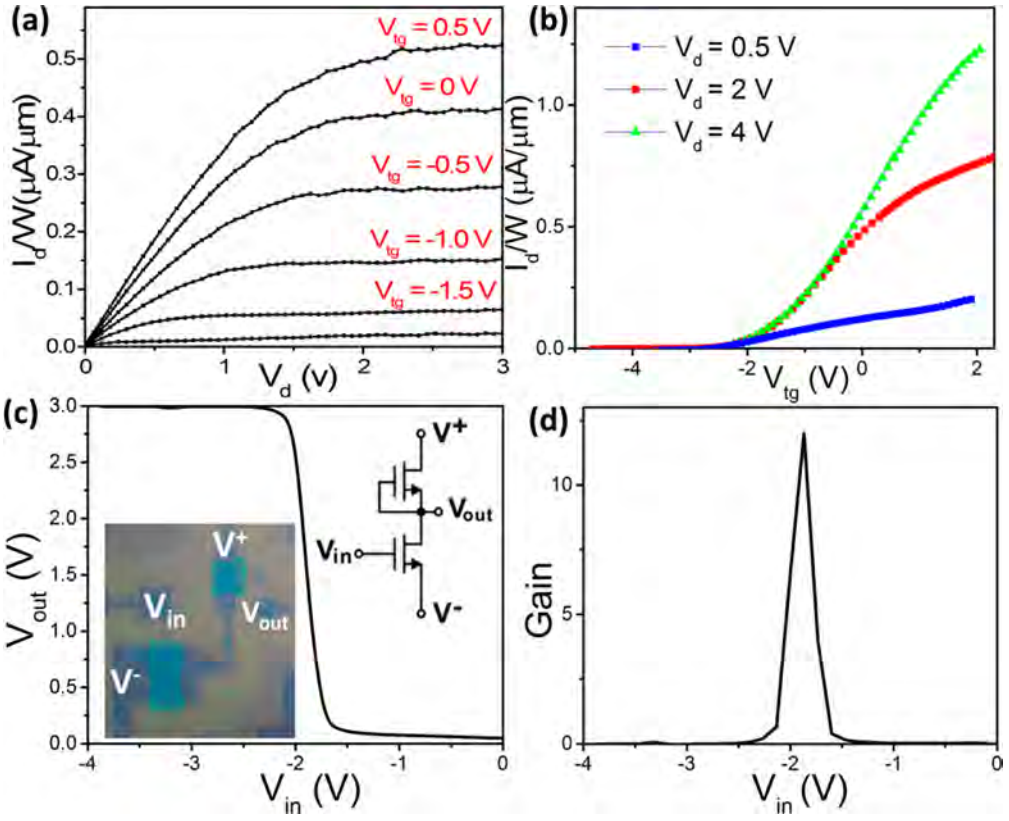

Figure 3. (a) Output characteristics (I_d vs V_d) and (b) transfer characteristics (I_d vs V_{tg}) of top-gated MoS_2 transistor with Al_2O_3 as top gate dielectric, graphene as source, drain, and gate electrodes. V_{tg} is the top gate voltage. (c) Output voltage as a function of the input voltage for a MoS_2−G logic inverter. Optical image (inset at lower left corner) and schematic of the electronic circuit (inset at upper right corner) for the inverter. (d) The gain of the inverter, which is larger than 12.

gate of the transistor, while the MoS_2 channels were protected by the Al_2O_3 etch-stop layer, see Figure 1c, right panel. The sample was then cleaned by acetone and annealed to remove PMMA residues. (Alignment accuracy of this process and alternate lithography methods for EBL is discussed in Supporting Information). By using patterned etch stop with specific design, we are able to make any 2D heterojunction in wafer scale. This pave the way for large-scale application of 2D heterojunction devices, such as heterojunction laser, photodetector, heterojunction bipolar transistors, tunneling FET, high-electron-mobility-transistor, etc.

Schematic and optical micrograph images of a dual gate FET are shown in Figure 1c (right panel) and Figure 1d, respectively. This device (MoS_2−G FET) has MoS_2 as channel, ALD Al_2O_3 as top gate dielectric, and graphene as source, drain and gate electrodes (connected to metal pads for measurement) and SiO_2/Si as back gate. In Figure 1d, the single layer graphene and single layer MoS_2 can be clearly distinguished through the optical contrast because of the thin material structure and interference effect between the graphene and MoS_2 with the SiO_2/Si substrate underneath with orange background for SiO_2, bright blue squares for Al_2O_3, blue for MoS_2, and grayish purple for graphene. In the AFM image of the channel region, Figure 1d right panel, the signature wrinkles on the CVD graphene can be clearly seen. The surface of the low-temperature ALD Al_2O_3 layer is uniform and free of pinholes, with a dielectric thickness of 20 nm as measured by AFM. Using this large-scale hybrid structure process, we have successfully fabricated various devices and integrated circuits on a single chip, shown in Figure 1e. FETs, Hall bars, and transmission line method (TLM) structures were made to characterize the material properties and device performance, while inverters and NAND gates demonstrate the scalability and the potential of this technology for mass production. On the same chip, a batch of control devices and circuits were also fabricated with 15 nm Ti/45 nm Au metal stacks as electrodes (MoS_2−Ti devices and circuits), shown in red dashed-line rectangles in Figure 1e. We chose Ti here because it is the most commonly used metal for MoS_2 FET research[1,30] and has been proposed as excellent metal contacts for n-type MoS_2 FET in previous theoretical papers.[31,32] The MoS_2−Ti devices and circuits were also fabricated with Al_2O_3 as top dielectric layers and graphene as top gate in order to eliminate the effect from high-κ dielectric and top/back gate couplings while investigating the role of the source drain contacts. This is the first time large-scale graphene/MoS_2 hybrid 2D electronics, both grown using CVD methods in their single-layer form, were fabricated using a CMOS-compatible, fully integrated process.

All the fabricated devices and circuits were measured in a vacuum probe station (Lakeshore cryogenics) at a pressure of ~3 × 10^{-6} Torr. During the back-gate sweep measurements, the top gates are grounded to avoid the coupling between top and back gates.[33] We studied about 50 devices that showed highly reproducible performance. Representative back-gated transport characteristics of the MoS_2−G transistor are shown in Figure 2a,c with a device channel length of 12 μm and width of 20 μm. Figure 2a shows the output performance (I_{ds} vs V_{ds}) of the devices. The current is linear with small source-drain biases (10 meV), indicating that the contact between graphene and MoS_2 is ohmic. The symmetry of the current with respect to the origin at positive and negative biases (inset of Figure 2a) further verifies the ohmic

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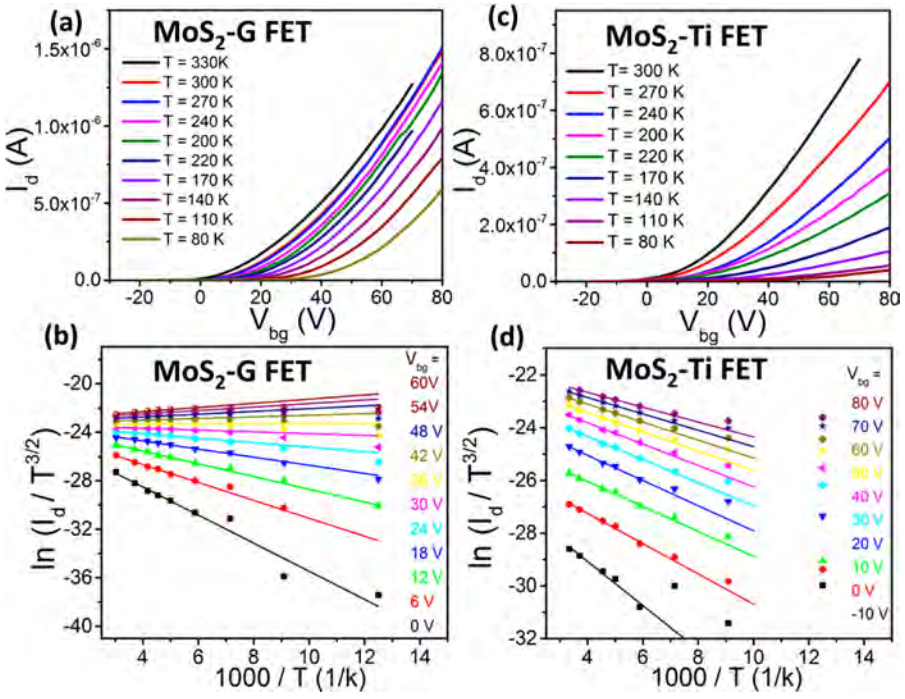

Figure 4. Temperature-dependent transport, that is, I_d–V_{bg} curves at various temperatures: (a,b) MoS_2–G FET, (c,d) MoS_2–Ti FET. The source drain bias for both structures are 0.5 V during measurement. In (b,d) we show the linear fit of Arrhenius plot $\ln(I_d/T^{3/2})$ vs $1000/T$.

nature of the contacts. The transfer characteristics (I_{ds} vs V_{bg}) of MoS_2–G and MoS_2–Ti FETs (used as control devices with exactly the same geometry) are shown in log scale in Figure 2b,d, respectively. They both have on/off ratios larger than 10^6. The current density is 8 μA/μm at V_d = 7 V, V_{bg} = 60 V for MoS_2–G FET, about 12 times higher than that of MoS_2–Ti, because of the lower barrier between MoS_2 and graphene than that between MoS_2 and Ti. The transconductance per channel width ($g_m/W = dI_d/dV_{bg}/W$) of MoS_2–G is 0.15 μS/μm with 300 nm SiO_2 back gate oxide, more than 1 order of magnitude higher than that of MoS_2–Ti structures. The field effect mobilities calculated from the transfer characteristics are shown in Figure 2c. The field effect mobility is calculated using expression $\mu = [dI_d/dV_{bg}] \times [L/(WC_{ox}V_d)]$, where V_{bg} and V_d are the back-gate voltage and source-drain voltage, L and W are the channel length and width, and C_{ox} (11 nF) is the capacitance per unit area between the channel and the back gate (calculated from 300 nm SiO_2).The mobility of MoS_2 in MoS_2–G structures reaches the peak value of 17 $cm^2/(V\ s)$, while the MoS_2–Ti structure has a peak mobility of only about 1.8 $cm^2/(V\ s)$. This value could be further improved by elimination of trapping states and by using substrates such as boron nitride (BN) to reduce surface roughness and block substrate charge.[34] The measured I–V characteristics are fitted to a classic drift-diffusion model to extract the contact resistance for MoS_2–G and MoS_2–Ti FETs. The effective gate voltage V_{gs_eff} and source drain voltage V_{ds_eff} are given by $V_{gs-eff} = V_{gs} - R_sI_{ds}$, $V_{ds-eff} = V_{ds} - (R_s + R_d)I_{ds}$, with R_s, R_d the parasitic series source/drain contact resistances. The contact resistance is 0.1 and 1 kΩ mm for MoS_2–G and MoS_2–Ti, respectively. The single layer MoS_2 has larger bandgap than multilayer MoS_2 and the CVD sample has lower doping concentration than flakes exfoliated from the mineral. These result in lower density of state, making it more difficult to achieve good contacts to single layer CVD MoS_2 compared to multilayer flakes, as was also found in other literature reports.[3,35] More work is needed to further decrease the contact resistance, especially by degenerate doping of the MoS_2 layer. The MoS_2–G contact in the present work exhibits a state-of-the-art contact resistance between CVD MoS_2 and CVD graphene. The use of graphene as contacts for MoS_2 FETs, as discussed above, provides 10 times lower contact resistance and 10 times higher on-current and field-effect mobility than conventional MoS_2-metal contacts. In addition, it has been shown in previous work that graphene-MoS_2 junction is robust with strain of 1.5%.[9] This new contact scheme is expected to also benefit flexible electronics, where most device failures are typically related to crack formation in the metal electrodes.[9,36] In addition, graphene can act as transparent electrode for MoS_2 optical devices, because the sputtering process commonly used in the deposition of transparent metal indium tin oxide (ITO) is not compatible with fragile single-layer MoS_2.

The top-gated performance of the MoS_2–G transistors is plotted in Figure 3. The output characteristics show a linear current behavior at low drain bias voltages (0.5 eV), and current saturation at higher biases. In the linear regime at small source-drain voltages, the current is proportional to V_{ds}, indicating that the source and drain electrodes made of graphene form ohmic contact with MoS_2. The current saturates at higher drain bias ($V_{ds} > V_{tg} - V_t$, where the V_{tg} is the top-gate voltage while V_t is the threshold voltage of the device) due to the formation of depletion region on the drain side of the gate, as is typical of long channel MOSFETs. The onset for current saturation because of channel pinch-off follows the relationship $V_{ds} > V_{tg} - V_t$ with V_t = −1.7 V. The transfer characteristics are shown in Figure 3b. The results show the on–off ratio of the device is larger than 10^3. The transconductance in this device is 0.5 μS/μm at V_d = 7 V (Figure S3a, Supporting Information). The transconductance drops at the high gate voltage region, because of the access resistance. Further development of self-aligned technology or doping of the access regions could help solve this problem. The subthreshold swing is 150 mV (Figure S3b, Supporting Information), corresponding to a midgap interface trap density value of 2.7 ×

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10^{12} cm^{-2} eV^{-1}, using the value of C_{ox} calculated from 20 nm thick Al_2O_3 with a dielectric constant of 7.

Using the technology described above, we have built several basic integrated logic circuits. For example, a fully integrated inverter was fabricated in depletion mode transistor resistor configuration, using two MoS_2−G FETs, shown in Figure 3c. The two transistors act as a switching and a load resistor, respectively (see schematic diagram, Figure 3c inset). The output characteristics of the inverter are shown in Figure 3c. A low voltage of −4 V represents a logic state 0 and a voltage close to 0 V represents logic state 1. The inverter is able to be operated under a supply voltage (V_{dd}) of 3 V, as shown in Figure 3c. The voltage gain is close to 12, as shown in Figure 3d. This is the first demonstration of logic circuits using CVD-grown 2D heterostructures that is mass producible. Further improvement in device and circuit performance can be achieved by changing the dielectric layers to insulating 2D crystals such as hexagonal boron nitride or 2D oxides.[9−11,37−39]

The results from our FETs and circuits demonstrate the advantages of graphene as a contact material for 2D electronic systems. They also highlight the key role of the interfacial barrier height between the active channel and electrodes in device performance. In the following, we give a systematic comparison of the barrier between MoS_2/graphene and that between MoS_2−Ti in the control structure. To study the barrier height we have characterized the transport properties at different temperatures and fitted the data using a thermionic emission model (Figure 4). The current through a Schottky barrier into 2D material can be described using the 2D thermal emission equation

$$I_d = AT^{3/2}\exp\left(\frac{-q\varphi_B}{k_BT}\right)\left[\exp\left(\frac{qV_d}{nk_BT}\right) - 1\right]$$
$$= I_s\left[\exp\left(\frac{qV_d}{nk_BT}\right) - 1\right]$$

where I_d is the current, A is Richardson's constant, T is the temperature, φ_B is the barrier between the metal and semiconductor, k_B is the Boltzmann constant, q is the electronic charge, V_d is the source to drain bias, and n is the nonideal factor of the Schottky diode. The power law of $T^{3/2}$ comes from the Boltzmann carrier distribution and the thermal velocity. It is less than T^2 commonly found in a 3D system because of the constant value of the density-of-states in a 2D system.[40] n is calculated by fitting the I_d versus V_d curves using the expression $I_d = I_s[\exp(q(V_d - I_dR_s)/nk_BT) - 1]$, where R_s is the series resistance from the device channel (see details in Supporting Information). The current as a function of back gate bias for the MoS_2−G FET at different temperatures is shown in Figure 4a and that for the MoS_2−Ti FET in Figure 4c. For both structures, the current decreases as temperature decreases. However, the temperature dependence in MoS_2−G is much weaker than that of MoS_2−Ti, indicating a smaller thermal emission barrier in the MoS_2−G structure. In MoS_2−G, the threshold voltage shifts to more positive values with decreasing temperature (Figure S4, Supporting Information) and the mobility remains almost constant with the same gate overdrive $V_{bg} - V_t$. In the MoS_2−Ti structure, the threshold voltage does not change, while the transconductance or mobility decreases with decreasing temperature (see Figure S5, Supporting Information). To determine the Schottky barrier height (SBH, denoted by φ_B), we plot $\ln(I_d/T^{3/2})$ versus $1000/T$ for various values of V_{bg} as shown in Figure 4b,d for MoS_2−G and MoS_2−Ti, respectively. When $V_d \geq 3k_BT/q$,

$$\ln\left(\frac{I_d}{T^{3/2}}\right) = -\frac{q\left(\varphi_B - \frac{V_d}{n}\right)}{k_BT} + \ln(A)$$

The effective SBH can be extracted from the slope of $\ln(I_d/T^{3/2}) - 1/T$ and the n value we obtain from fitting the I_d vs V_d curves. The resulting values are shown in Figure 5. The excellent fitting over all the temperatures is evidenced by the small error bar values.

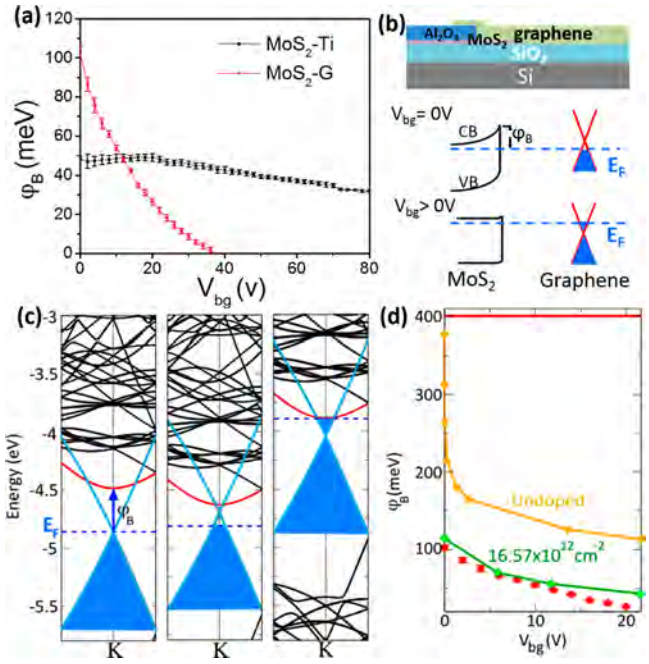

Figure 5. (a) Schottky barrier height φ_B (in meV) and corresponding error bars, as a function of the gate bias V_{bg} (in V) for CVD grown MoS_2−G and MoS_2−Ti junctions. (b) Experimental setup used (upper panel) and schematic band diagram of MoS_2/G heterostructure at V_{bg} = 0 and $V_{bg} > 0$ (bottom panel). The corresponding edges of the valence band (VB) and the conduction band (CB) are shown, with E_F marked by the dashed line. (c) Calculated band structures of MoS_2/graphene interface at zero bias and doping (left), zero bias with finite doping concentration (11.05×10^{12} cm^{-2}) (middle) and 80 V back gate bias at the same doping (right). φ_B is indicated by the vertical arrow pointing from E_F to the CB minimum at the K point. The relevant graphene and MoS_2 states are shown by blue and red lines, respectively. (d) Calculated φ_B (in meV) as a function of the bias voltage V_{bg} (in V) at different doping levels. The horizontal red line at 400 meV shows the value of the φ_B expected from the difference between the work function of graphene (4.5 eV) and the electron affinity of MoS_2 (~4.1 eV). The red dots show the experimental results from (a).

In MoS_2−G, φ_B decreases dramatically from 110 to 0 meV with the back gate voltage changing from 0 to 35 V, as shown in Figure 5a. Previous studies have shown MoS_2/graphene Schottky barriers ranging from 22 to 260 meV, depending on different gate voltage and sample preparation conditions.[10,37] The barrier height in MoS_2−Ti has relatively weak dependence with back gate voltage, changing from 50 to 40 meV with back gate changing from 0 to 80 V, as shown in Figure 5a. For an ideal metal semiconductor contact, φ_B is determined by the difference between the work function of the metal (W_m), the affinity of the semiconductor (χ_s) and surface potential (ϕ_s), that is, $\varphi_B = W_m -$

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$\chi_s + \phi_s$. The change of φ_B in MoS_2−G comes from changes in both W_m and ϕ_s, as shown schematically in Figure 5b. In MoS_2−Ti, the W_m modulation is very limited, and the change in SBH is believed to come from the modulation of midgap interface states that impact ϕ_s, just like in conventional metal−semiconductor junctions.

The work function of graphene can be modulated by electric field, following the expression:

$$W_m = E_F = -\mathrm{sgn}(n_0)\hbar\nu_F\sqrt{\pi|n_0|}, \qquad n_0 = q(V_{bg} - V_t)$$

where n_0 is the carrier concentration in graphene, $\hbar$ Planck's constant, and ν_F the Fermi velocity.[41] It was already found in the past that a change in the value of V_{bg} by 30 V with 300 nm SiO_2 as back gate dielectric can cause a change of around 200 mV in graphene work function,[41] which is consistent with the change in the Schottky barrier height observed in our experimental data. As a result of this modulation, when the back gate voltage is larger than 35 V, the Schottky barrier height between MoS_2 and graphene is zero and an ohmic contact forms at the MoS_2 and graphene junction. Graphene outperforms Ti to contact MoS_2 with large carrier density which can be achieved using electronic doping or chemical doping.[43] The finite density of states and the tunability of its work function make graphene capable to form excellent contacts with MoS_2 and other semiconductors, offering new opportunities to design contact and to engineer junction interfaces.[42]

To elucidate some of the features of the MoS_2−G heterostructure, we performed first-principles calculations using density functional theory (see Methods section for further details). Figure 5c shows the calculated band structure of the MoS_2−G heterostructure for different doping and electric bias. In these calculations, we have considered only contact barriers which arise in the direction perpendicular to the 2D layers. The MoS_2−G heterostructure has metallic character with the graphene Dirac cone from the dispersion of the p_z states falling within the MoS_2 band gap. The polarization of the electronic charge at the interface (see Figure S7 in Supporting Information) is stronger in graphene interfaces than in late transition metals,[41] which will be beneficial to the transfer of electrons from MoS_2 to graphene. Because of the very small density of states near the Fermi level (around the graphene Dirac point), the behavior of the device is sensitive to the position of E_F inside of the band gap, which can be changed by electronic doping or external electric fields. At conditions of zero external bias and no doping (left panel in Figure 5c), E_F is at the Dirac point and corresponds to small charge transfer (~0.01 electrons per cell from MoS_2 to graphene) and relatively weak interactions (~55 meV per C atom). At finite doping (middle panel in Figure 5c) or electric fields (right panel in Figure 5c), E_F is shifted away from the Dirac point, which changes the magnitude of the Schottky barrier height φ_B. In this case, the barrier is given by the difference between the Fermi level of the combined system and the conduction band minimum of MoS_2 at the k-point in the Brillouin zone. The results of barrier height change as a function of the external bias are shown in Figure 5d: At no doping and zero electric bias, the barrier height is 385 meV, close to the value of 400 meV obtained by simply calculating the difference between the graphene work function and the electron affinity of MoS_2. In the real system, a small amount of doping will shift the value of φ_B significantly from this value. When an external electric field is applied, φ_B decreases monotonically with increasing values of the bias. The amount by which φ_B changes depends on the level of doping. The strong dependence of the value of φ_B on the gate voltage, in the range $0 < V_{bg} < 2$ V is due to the very low density of states near the graphene Dirac point, as mentioned above, which results in large shift of the Fermi level for small amount of induced charge. For values of $V_{bg} > 6$ V, the change in φ_B is smaller, and its slope is almost independent of the doping level at high concentrations (~10^{13} cm^{-2}, see Figure S8 in Supporting Information for different values of doping).

In summary, a novel 2D electronic system using heterostructures of single-layer MoS_2 and graphene has been demonstrated where MoS_2 serves as the channel material and graphene is used as both the ohmic and gate contacts, and the interconnects for the 2D electronic system. This technology represents the first large-scale platform for constructing electronics based on van der Waals heterostructures of 2D material monolayers. Both MoS_2 and graphene monolayers were grown using low-cost CVD methods, which are easily scalable to any size on arbitrary substrates. This work lays the foundation for a scalable all-2D-material electronics platform capable of taking full advantage of the mechanical flexibility and electrostatic integrity offered by monolayer electronic materials for applications in flexible and transparent electronics. Our systematic analysis of using graphene as contact material to interface with 2D semiconductors (in this study MoS_2) for effective carrier injection into the channel, demonstrates that the tunable Fermi level offers unprecedented flexibility for matching the work-function of the contacts with the channel. Combining the many advantages of graphene in high frequency electronics,[44−46] and its potential use as a new interconnect material superior to metals[42,47] at the nanometer scale,[48] the technological framework demonstrated in this work opens the door to many new opportunities for designing novel electronic systems.

Methods. *Low-T ALD.* The low-temperature ALD deposition of Al_2O_3 was performed on a commercial Savannah ALD system from Cambridge NanoTech at 100 °C using alternating cycles of H_2O and trimethylaluminum (TMA) as the precursors. The purge time between each cycle is 60 s to allow the full reaction.

AFM and Raman Spectroscopy. AFM for identifying the thin film thickness was performed on a Veeco Dimension 3100 system. Raman spectroscopy was performed with a 532 nm Nd:YAG laser. All optical micrographs were taken with a Zeiss Axio Imager.A1m microscope.

Device and Circuit Characterization. Device characterization was performed using an Agilent 4155C semiconductor parameter analyzer and a Lakeshore cryogenic probe station with micromanipulation probes. All measurements were done in vacuum (3×10^{-6} Torr) at room temperature.

First-Principles Electronic Structure Calculations. The calculations reported here are based on density functional theory calculations using the SIESTA code.[49] The generalized gradient approximation[50] and nonlocal van der Waals density functional[51] was used together with double-ς plus polarized basis set, and norm-conserving Troullier-Martins pseudopotentials[52] to represent the atomic cores. The resolution of the real-space grid used to calculate the Hartree and exchange-correlation contribution to the total energy was chosen to be equivalent to 150 Ry plane-wave cutoff. Atomic coordinates were allowed to relax using a conjugate-gradient algorithm until all forces were smaller in magnitude than 0.01 eV/Å. To simulate the interface between graphene and MoS_2 layers, supercells containing up to 488 atoms were constructed using a graphene supercell of 5×5 and a MoS_2 supercell of 4×4 that are approximately lattice matched in different stacking configurations. To avoid interactions between

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layer images the distance between periodic images of the structures along the direction perpendicular to the surface was always larger than 20 Å. The number of *k*-points was chosen according to the Monkhorst–Pack[53] scheme, and was set to the equivalent of a 47 × 47 × 1 grid in the primitive unit cell of graphene, which gives well-converged values for all the calculated properties. We used a Fermi–Dirac distribution with an electronic temperature of k_BT = 21 meV. The external electric field is introduced through a sawtooth-like electrostatic potential in the direction perpendicular to the MoS_2–G plane. The different doping levels are obtained by adding a certain amount of electrons to the system and imposing a compensating uniform background in order to converge the total energy and the long-range Coulomb interactions.[52,54]

■ ASSOCIATED CONTENT

Supporting Information

CVD growth of MoS_2 and single layer graphene, alignment accuracy of fabrication process, top gate performances of MoS_2–G FET, temperature-dependence of MoS_2–Ti and MoS_2–G FETs, calculation of *n* and R_s, and DFT calculation of graphene/MoS_2 interface. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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