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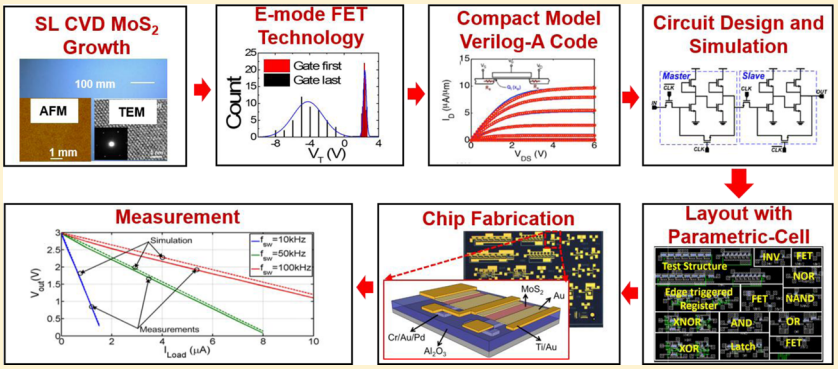
Design, Modeling, and Fabrication of Chemical Vapor Deposition Grown MoS_2 Circuits with E-Mode FETs for Large-Area Electronics

Lili Yu,[*,†] Dina El-Damak,[*,†] Ujwal Radhakrishna,[†] Xi Ling,[†] Ahmad Zubair,[†] Yuxuan Lin,[†] Yuhao Zhang,[†] Meng-Hsi Chuang,[‡] Yi-Hsien Lee,[‡] Dimitri Antoniadis,[†] Jing Kong,[†] Anantha Chandrakasan,[†] and Tomas Palacios[†]

[†]Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, Massachusetts 02139, United States

[‡]Materials Science and Engineering, National Tsing-Hua University, Hsinchu 30013, Taiwan

Supporting Information



ABSTRACT: Two-dimensional electronics based on single-layer (SL) MoS_2 offers significant advantages for realizing large-scale flexible systems owing to its ultrathin nature, good transport properties, and stable crystalline structure. In this work, we utilize a gate first process technology for the fabrication of highly uniform enhancement mode FETs with large mobility and excellent subthreshold swing. To enable large-scale MoS_2 circuit, we also develop Verilog-A compact models that accurately predict the performance of the fabricated MoS_2 FETs as well as a parametrized layout cell for the FET to facilitate the design and layout process using computer-aided design (CAD) tools. Using this CAD flow, we designed combinational logic gates and sequential circuits (AND, OR, NAND, NOR, XNOR, latch, edge-triggered register) as well as switched capacitor dc−dc converter, which were then fabricated using the proposed flow showing excellent performance. The fabricated integrated circuits constitute the basis of a standard cell digital library that is crucial for electronic circuit design using hardware description languages. The proposed design flow provides a platform for the co-optimization of the device fabrication technology and circuits design for future ubiquitous flexible and transparent electronics using two-dimensional materials.

KEYWORDS: *Transition metal dichalcogenides, molybdenum disulfide, chemical vapor deposition, computer-aided design flow, digital circuits, power management circuits*

The growing interest in foldable and lightweight electronic systems has helped the development of different flexible semiconductor technologies that have the potential to replace rigid silicon. Flexible materials can significantly improve the design of implantable and wearable devices, as well as a new generation of prosthetic limbs and robots.[1] Flexible electronics can also enable smart textiles with embedded sensors for monitoring various vital signals of the human body.[2] Despite the great interest in developing transistors on flexible substrates, most of the approaches pursued so far have very limited performance in terms of mobility and yield or their fabrication process is very complex. For example, organic semiconductors have typical carrier mobilities below than 1 $cm^2/(V\ s)$,[3] and amorphous metal oxides show performance shift under illumination or thermal stress.[4,5] Carbon nanotube-based electronics shows improved performance, however it still suffers from metallic impure tubes, which result in complex and additional fabrication processing steps.[6,7] On the other hand, few-layer-thick molybdenum disulfide (MoS_2) has the potential to overcome many of these challenges.[8−11] Strong intralayer covalent bonds confer MoS_2 crystals excellent mechanical strength, thermal stability, and a surface free of dangling bonds. At the same time, single layers of MoS_2 can be grown over large areas by chemical vapor deposition (CVD) and their wide bandgap (1.8 eV), high carrier mobility (120 $cm^2/(V\ s)$ at room temperature; 34 000 $cm^2/(V\ s)$ for 6L exfoliated MoS_2 at low temperature; 1020 $cm^2/(V\ s)$ for 1L CVD monolayer at

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low temperature),[12] planar nature and mechanical flexibility make it an excellent candidate for the fabrication of transistors for both analog and digital circuits. Despite the promising characteristics of MoS_2, applications so far have been limited to single or few devices due to the many challenges associated with the uniformity and yield control in both material growth and device technology, as well as lack of an enhancement-mode (E-mode) transistor technology.[10,13,14]

In this work, we push the MoS_2 technology forward by demonstrating E-Mode transistors, compact modeling and a custom computer-aided design (CAD) flow to enable complex circuits for the first time. First, we present a gate-first process where all the passive components are fabricated before the MoS_2 transfer. This approach minimizes the fixed-charge in the gate dielectric of MoS_2 transistors. This results in MoS_2 transistors with small subthreshold voltage swing and positive threshold voltage and tight statistical distribution, which is essential for the successful design of multistage cascaded circuits. Second, compact virtual source device models are used to capture the different regions of device performance (subthreshold, linear, saturation) and to predict future FET performance as the fabrication process evolves. Third, we develop a CAD flow for the design, simulation, and layout of MoS_2-based circuits, using an industry-standard IC design environment. A variety of combinational (inverter, NAND, NOR, AND, OR, XOR, XNOR) and sequential logic circuits (latch, edge-triggered register) as well as switched capacitor DC-DC converter have been designed and characterized showing correct functionality. With the demonstrated fabrication technology, modeling, and computer-aided design flow, we provide a platform for the co-optimization of circuits and devices using MoS_2 while the fabricated circuits shows the great promise of the technology for realizing complex systems.

The design of electronic circuits using new materials like MoS_2 is often based on intuition, and the performance evaluation is conducted only after fabrication. Thus, researchers in emerging fields are able to take only limited advantage of state-of-the-art CAD software. A CAD flow typically includes physical or empirical models of the active and passive components, a circuit simulator for performance evaluation, parametrized layout cells, as well as verification tools for checking that the layout is compliant with design rules (such as metal spacing) as well as for comparing the layout versus the schematic. Thus, the CAD flow leads to a significant reduction in the time and consequently the cost of fabrication of advanced chips.

In order to enable the fabrication of large scale flexible systems using MoS_2, we combined our device technology with a CAD flow for the fabrication of MoS_2-based systems as shown in Figure 1. On the device development side, the flow starts with the growth of MoS_2 using chemical vapor deposition, followed by device fabrication and characterization. The CAD flow includes: (1) compact models of MoS_2 devices, (2) schematic design based on simulation results, (3) layout with parametrized cells using industry-standard IC design environment. Then, the full chip layout is exported in graphic database system (GDS) format for mask generation and chip fabrication is performed. This design flow allows for technology design co-optimization to realize the full potential of such emerging technology. It allows for capturing the impact of the device parameters on the circuit performance, speeding up the layout process, reducing the number of iterations for system

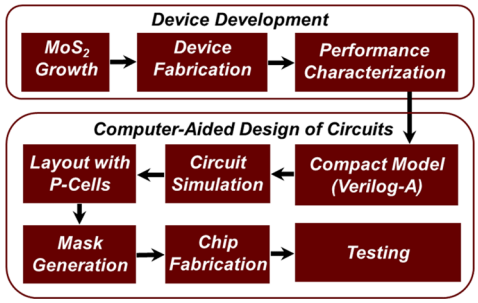

Figure 1. Design flow for large-scale MoS_2 integrated circuits.

development, and exploring the potential improvements on the system level with the predicted next generation device.

High-quality and large-area MoS_2 monolayers were obtained using scalable chemical vapor deposition (CVD) growth with the seeding promoter of perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS) on SiO_2/Si substrate (growth method details can be found in Supporting Information).[15,16] An optical image of as-grown CVD MoS_2 (Supporting Information, Figure S1) demonstrates good uniformity and a high coverage approaching 100%. Atomic force microscopy (AFM) and transmission electron microscopy (TEM) evidenced the high quality of the CVD MoS_2 monolayer.

The fabrication process of the transistors starts with cleaning a separate target SiO_2/Si substrate using nanostrip (Cyantek KMG) and hydrochloric acid (HCl) (Figure 2a). The transistor

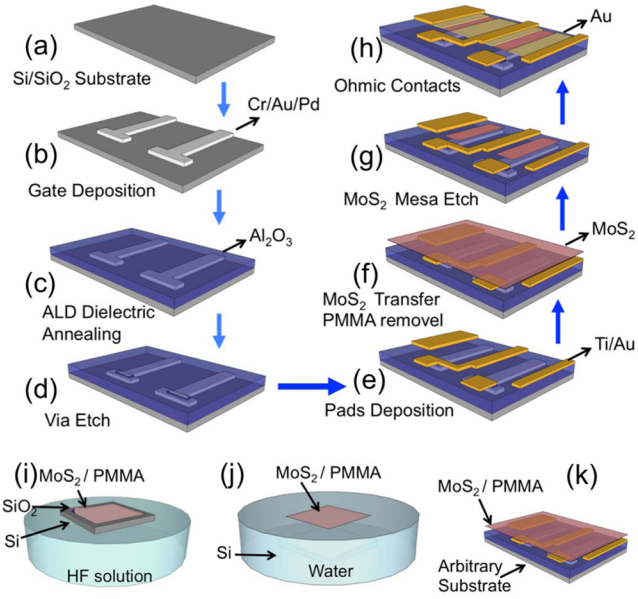

Figure 2. Fabrication process of an inverter (a–h) and transfer process of large area single layer MoS_2 (i–k).

gate is then formed using a stack of 5 nm chromium (Cr), 30 nm gold (Au), and 30 nm palladium (Pd) after that gate patterning is performed using photolithography (Figure 2b). The gate metal stacks are chosen for best combination of adhesion, conductivity, and high work function. A 30 nm thick aluminum oxide (Al_2O_3) layer deposited by atomic layer deposition (ALD) is used as gate dielectric (Figure 2c). Via hole is patterned based on the circuit layout, followed by etching using reactive ion etching (Figure 2d). Contact pads made of 5 nm titanium (Ti)/90 nm Au metal stack are

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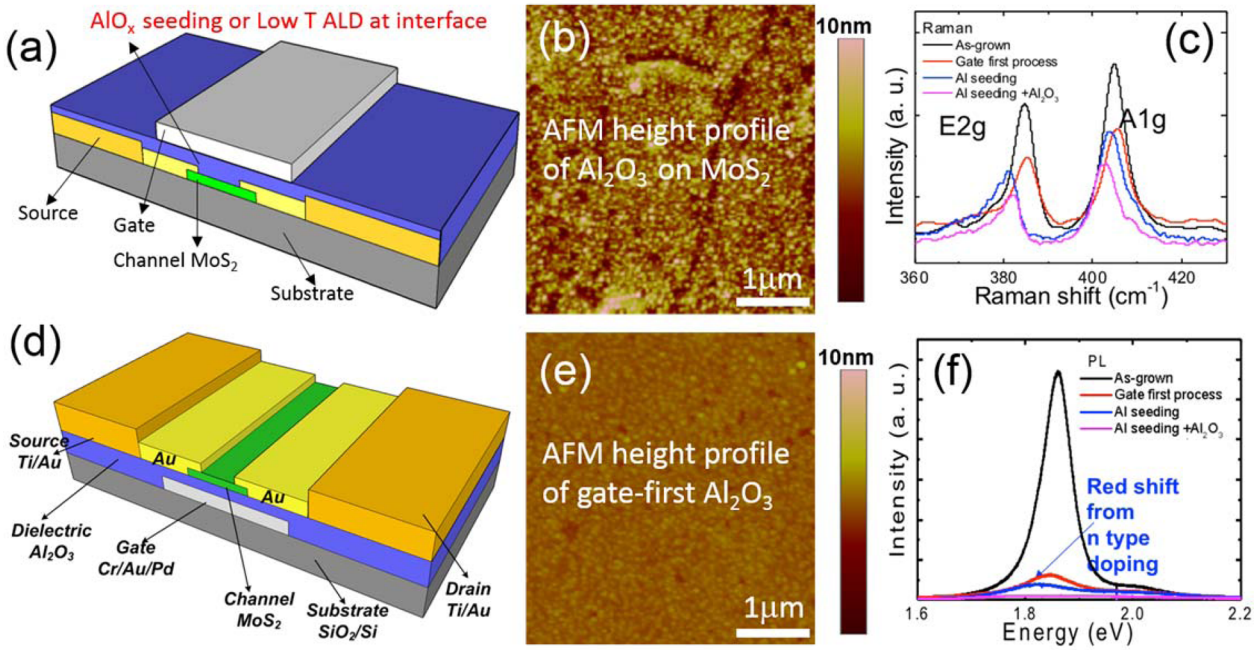

Figure 3. Three-dimensional image of conventional gate-last (a) and gate-first (d) process of transistor. AFM image of dieletric of Al_2O_3 deposited on MoS_2 in gate-last process (b) and Al_2O_3 deposited on substrate in gate-first process (e), pinholes can be identified in (b), which can cause device variation, material degradation, and early breakdown of dielectric layer. (c) Raman and (f) photoluminescence (PL) spectra for a single MoS_2 layer right after CVD growth and after different fabrication steps. The strong PL intensity and the characteristic Raman peak of the as-grown sample (black line) indicate good quality of single layer MoS_2. After the deposition of the Al seeding layer, the positive fixed charge n-dopes the MoS_2, as evidenced by the redshift of A_{1g} Raman peak and PL signal. The ALD layer shifts them even further. A higher electron density introduces a larger intensity of the trion peak that has lower energy than the exciton, shown as a redshift of PL peak. The highly suppressed PL intensity after Al deposition and ALD deposition also indicates degradation of MoS_2 quality. In comparison, there is no shift in Raman or PL peak in MoS_2 after gate first process. The lower intensity of the PL signal is mainly attributed to exposure to polymer during transfer process.

deposited before the MoS_2 transfer (Figure 2e). As-grown MoS_2 CVD sample is coated with poly(methyl methacrylate) (PMMA) as supporting layer and soaked in diluted HF solution (Figure 2i). The SiO_2 layer underneath the MoS_2 is etched away and the MoS_2/PMMA stack is then released (Figure 2j) and transferred to the prefabricated target substrate (Figures 2f,k). O_2 plasma is then used to isolate the MoS_2 transistor channels (Figure 2g). Ohmic contacts are formed by depositing a 90 nm Au layer (Figure 2h).

For MoS_2 FETs fabricated with the conventional gate-last process (Figure 3a), dielectric integration is usually conducted at low temperature[8] or assisted by seeding layer (oxided thin metal layer or high energy gas),[17,18] both resulting in fixed charge and trap states inside the dielectric or at the interface, degrading the mobility and causing negative shift in V_T. The AFM image of the interface (Figure 3b) shows rough surface and pinhole in the dielectric, and the Raman (Figure 3c) and PL (Figure 3f) peaks of the MoS_2 shifted because of the n-type doping introduced from the fixed charge in dielectric. On the other hand, the gate-first process (Figure 3d) described earlier improves the interface quality with respect to a gate-last process as evidenced by AFM, Raman, and PL characterization (Figure 3e,c,f).

By using this gate-first process, all the critical components are fabricated before the MoS_2 transfer step. In Figure 4a, MoS_2 FETs with gate-first technology show much more positive V_T, 10× larger on-state current, 1000× smaller off-state current, and steeper subthreshold slope in comparison with gate-last based FETs. The E-mode device output characteristics is shown in Figure 4b. These devices have high on/off current ratio, large

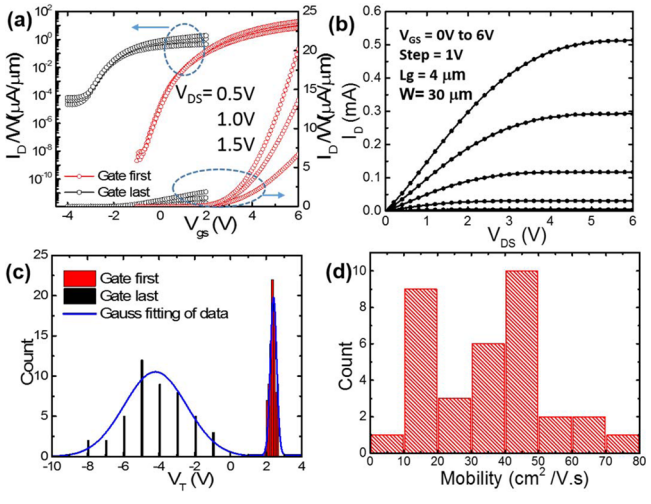

Figure 4. (a) Transfer characteristics in linear (right y-axis) and log scale (left y-axis) and (b) output characteristics shows good saturation and immunity to channel length modulation. W = 30 μm, L_g = 4 μm. (c) Statistics of V_T of MoS_2 FETs (channel length of 2 μm from different fabrication technologies. (d) Field-effect mobility distribution of single layer MoS_2 FET using gate-first process. The high mobility of single layer CVD MoS_2 is preserved from gate-first process.

on-current, and excellent saturation. Very limited channel length modulation is observed in these devices for a gate length of 4 μm that is crucial for high gain circuits. In addition, the gate-first process achieves close to 100% yield (on/off ration $>10^4$ and $V_T > 0$ V) of a single transistor across a test chip with

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more than 200 FETs. Uniformity and repeatability of transistor performance are very critical to multistage large area complex integrated circuits. Thus, it is more challenging to realize complex integrated circuits based on CVD single layer MoS_2. compared to using single crystal MoS_2 flakes, because of the variation introduced by the multicrystalline nature of CVD MoS_2.[15] The gate first process substantially improves the transistor uniformity. Statistical study of the transistor performance shows that gate-first devices have an average V_T of 2.41 V with standard deviation of 0.17 V while those from gate-last process have average V_T of −4.20 V and much larger standard deviation of 1.75 V (Figure 4c). The positive and tight distribution of V_T is critical for designing cascaded circuit with large noise margin. The mobility of E-mode MoS_2 FETs have been extracted from tens of FETs (Figures 4d). The high room-temperature mobility (as high as 80 $cm^2/V{\cdot}s$) shows the small charge impurity scattering from the interface of the dielectric. The statistic distribution of device subthreshold swings also confirms the excellent quality and interface of the dielectric (Supporting Information, Figure S3).

After the device characterization, we utilize the long channel version of the MIT virtual source (MVS) model (Figure 5a) to model the MoS_2 transistor based on the carrier transport physics in the device. The MVS model has a small number of device parameters with physical meanings, and the model has been validated with experimental results for traditional[19] and emerging semiconductors, such as gallium nitride[20] and graphene.[21] The model formulas are shown below

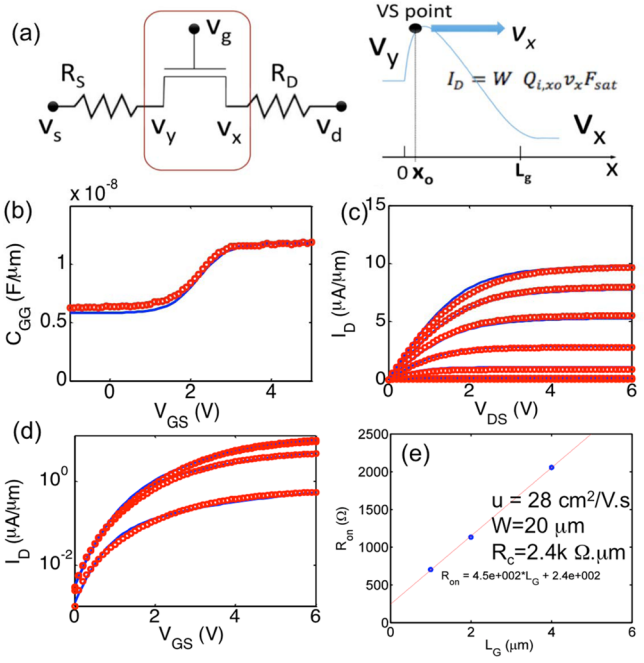

Figure 5. (a) The equivalent circuit model of the MVS approach adopted to capture the terminal characteristics of MoS_2 transistors. The band-profile along the device-channel in saturation is shown, indicating the virtual source point at which the current computation is done. (b) The electrostatic parameters are extracted from CV measurements and (c,d) the transport model is benchmarked against transfer characteristics of the device shown, where the model exhibits good accuracy against measurement data and is therefore suitable for meaningful circuit-design. (e) The values of parameters for the contact resistances are extracted from TLM measurements as shown.

$$\frac{I_D}{W} = \frac{(Q_{inv,s} + Q_{inv,d})}{2} v_{sat} F_{Vsat} \tag{1}$$

$$Q_{inv,s(d)} = 2C_g n\phi_t \ln\left(1 + \exp\left(\frac{(V_G - V_{S(D)}) - (V_T - \alpha\phi_t F_{f,S(D)})}{2n\phi_t}\right)\right)$$

$$F_{Vsat} = \frac{\frac{(Q_{inv,s} - Q_{inv,d})}{C_g V_{DSAT}}}{\left(1 + \frac{(Q_{inv,s} - Q_{inv,d})}{C_g V_{DSAT}}\right)^{1/\beta}}$$

$$\left(F_{Vsat} = \frac{(Q_{inv,s} - Q_{inv,d})}{C_g V_{DSAT}},\ \text{in mobility regime}\right) \tag{2}$$

$$Q_{S(D)} = \frac{2WL_g}{(Q_{inv,s}^2 - Q_{inv,d}^2)^2} \left[+(-)\frac{Q_{inv,s}^5 - Q_{inv,d}^5}{5} - (+)Q_{inv,d(s)}^2 \frac{Q_{inv,s}^3 - Q_{inv,d}^3}{3}\right];$$

$$V_{DSAT} = \frac{L_g v_{sat}}{\mu} \tag{3}$$

In the model, the current in the MoS_2 FET is calculated in terms of the areal-charge densities at the source and drain ends and the injected carrier velocity at the virtual source that is computed from gradual channel approximation (GCA) and current continuity as in eq 1, where W is the device width, Q_{is} and Q_{id} are the channel charges at source and drain, respectively, and v_{sat} is the saturation velocity of carriers. Transition from linear to saturation regime is governed by F_{Vsat}, which is obtained from closed-form solution to drift-diffusion (DD) transport in the MoS_2 channel as given in eq 2, where C_{invi} is the channel-to-gate capacitance, and β is an empirical parameter that can be obtained from experimental data. The device charges and hence capacitances are captured using expressions in eq 3, which are obtained from self-consistent solutions for charge partitioning that are consistent with carrier-transport. The terminal bias-dependent charges enable the model to be suitable for transient circuit simulations.

For the model fitting, the CV data is first used for estimating the electrostatic parameters of the device model, which is then used to self-consistently obtain the fits for carrier transport in the device. Device performance above/below threshold voltage (Figure 5d,e) are captured well with the model and the detailed model parameters can be found in the Supporting Information. The mobility and contact resistance from the model are consistent with the results from transmission line method (TLM) measurements. With the parameters extracted from the FETs, the MVS model is implemented in Verilog-A to enable circuit simulation as in the standard silicon ASIC design process.

In order to demonstrate the potential of our proposed design flow, we designed and fabricated various combinational (NAND, NOR, AND, OR, XOR, XNOR) and sequential circuits (latches, edge-triggered registers) using the MVS model of the MoS_2 FETs. These circuits form the basis to a standard cell library that can allow the synthesis of complex digital

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systems (such as a microprocessor) using hardware description languages. Moreover, we designed and fabricated switched capacitor dc−dc converter for voltage scaling using the proposed flow.

Logic gates are designed typically using pull-up and pull-down networks; the former is connected between the supply and the output node while the latter is connected between the output node and ground. In standard Si CMOS technology, the pull-up network is designed using pMOS transistors to allow rail-to-rail operation at a low power consumption.[22] If the output is logic high in such case, the transistors in the pull-up network will provide a low restive path to the supply, while the transistors in the pull-down network will be operating in deep subthreshold. Consequently, the logic level high in steady state is equal to V_{DD} less $I_{LeakPD}R_{PUH,}$ where I_{LeakPD} is the leakage current of the gate set by the pull-down network and R_{PUH} is the equivalent resistance of pull-up network while the output is high. Similarly, the logic level low in steady state is equal to $I_{LeakPU}R_{PDL}$ where I_{LeakPU} is the leakage current set by the pull-up network and R_{PDL} is the equivalent resistance of the pull-down network while the output is low. When the pull-up and the pull-down networks are designed using pMOS and nMOS devices, respectively, $I_{LeakPD}R_{PUH}$ and $I_{LeakPU}R_{PDL}$ are small enough such that the logic high and low levels are almost equal to V_{DD} and GND, respectively, while being highly independent of the transistor sizing.[22]

The existing MoS_2 technology lacks pMOS devices. MoS_2 is natively n-type as the material is subject to sulfur vacancies during the CVD growth process resulting in intrinsic electron concentration.[23] It is very challenging to fabricate pMOS from MoS_2 because of the trapping states, difficulty of doping MoS_2, and the lack of good contact methods to p-type MoS_2 transistors. In particular, current technology of high energy ion implantation for doping silicon is not applicable to MoS_2 because of its ultrathin structure. Consequently, the pull-up network in any logic gate made of MoS_2 has to be made of n-MOS.

In order to realize rail-to-rail output swing, high noise margin, narrow transition zone with minimal number of transistors, and one power supply, we implement the pull-up network with E-mode nMOS FET in subthreshold regime−gate to source voltage equals to zero. Figure 6 depicts the schematics (a,b), load-line plots (c,d), and voltage transfer characteristics (VTC) (e,f) of the (A) proposed topology and (B) diode-load nMOS only topology. The VTC of the inverter is inferred from the load-line plot through the intersection points of the $I-V$ curves of the transistors used for pull-up and pull-down after being transferred onto a common coordinate set.[24] For topology (A), most of the intersection points of the load-line occur at either low or high output levels, whereas either the bottom transistor is operating in the linear regime or the top transistor is at drain to source voltage below or close to subthreshold V_{DSAT}.[24] A higher gain and sharper transition are achieved with topology (A) as there are minimal number of intersection points in the load-line plot at the median input voltage range while the bottom transistor is in saturation. On the contrary for topology (B), most of the intersection points on the load-line plot occur while both transistors are in saturation above threshold, which results in low gain, low noise margin, and nonrail-to-rail output swing. It should be noted for topology (A) that the relative sizing of the transistors is critical as it determines the switching threshold, that is, it is ratioed logic.[22] Thus, there is a trade-off between the sizing of the gate

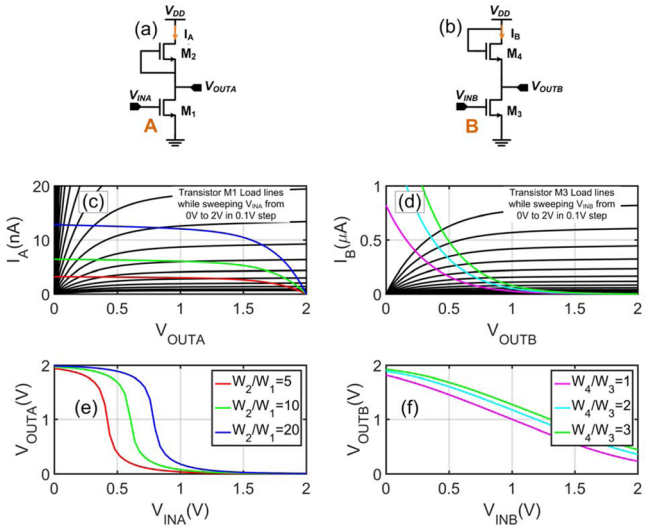

Figure 6. Circuit implementation and simulation results of inverters using a n-MOS MoS_2 FET as a load (A) in deep subthreshold operation (V_{GS} = zero) and (B) in diode-connected configuration. (a,b) Schematics of topology (A,B) respectively; (c,d) load-line plot for topology (A,B) respectively; (e,f) voltage transfer characteristics of the inverter using topology (A,B) respectively. All the simulation results are performed using the MVS model of the MoS_2 FETs using industry standard IC design environment.

and the noise margin. By sizing the top transistor with W/L that is 10 times larger than the bottom transistor, we were able to obtain a decent noise margin at a reasonable gate size. By realizing a rail-to-rail output swing, it is feasible to implement logic gates with cascaded stages.

In order to facilitate the mask generation for circuit fabrication, a custom technology library and a parametrized layout cell for the transistors are created in Cadence. The technology library file defines five main layers: (1) Mesa, to pattern the MoS_2; (2) Gate, to pattern the stack of Cr/Au/Pd; (3) Contact, to pattern Au; (4) Pad, to pattern the Ti/Au stack, and (5) Via, to define the holes used for creating connection from the gate layer to the pad layer. The parametrized layout cell allows the scaling of the width and length of the channel while maintaining a fixed overlap between the contacts and the MoS_2 (Supporting Information Figure S3). After the generation of the layout of each FET in a circuit, the placement and routing (using Pad and Gate layers) are done manually. Then, the full chip layout is exported in GDS format for mask fabrication. Figure 7 shows the layout and the optical photograph of the test chip with different device components, inverters, and multistage combinational (NAND, NOR, AND, OR, XOR, XNOR) and sequential circuits (latch, edge-

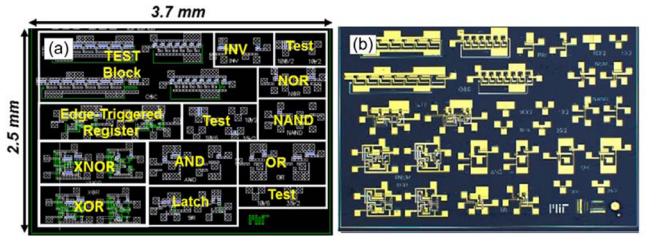

Figure 7. Layout and the optical photograph of fabricated test chip using the proposed flow.

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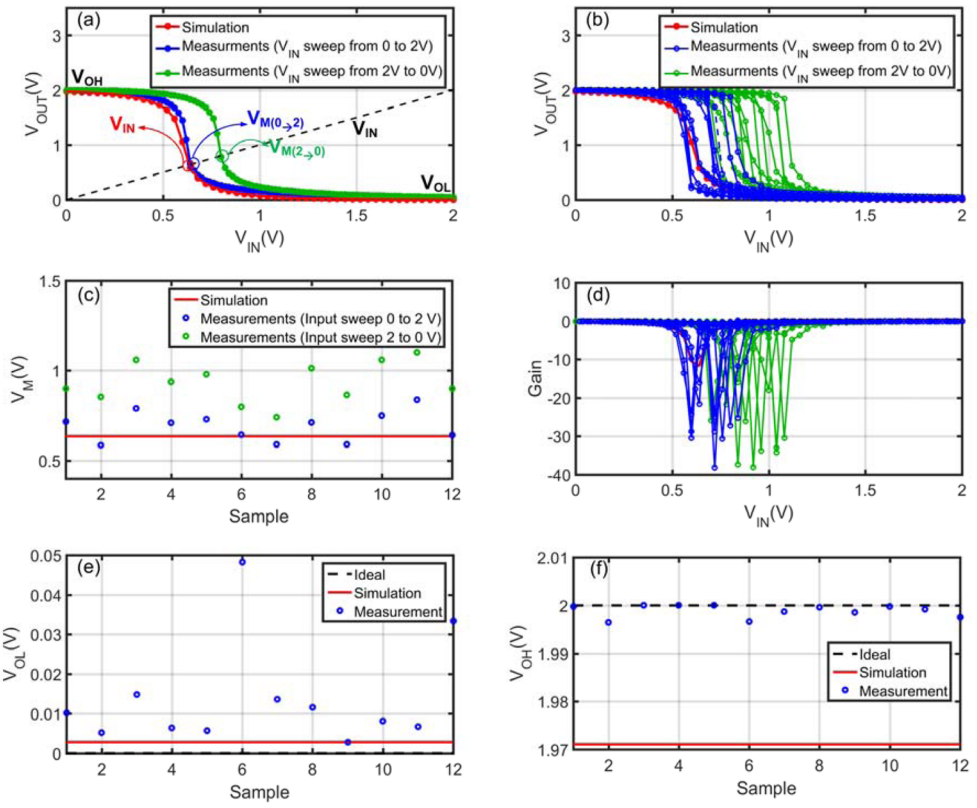

Figure 8. Simulation and measurements results of 12 inverter samples across 4 different chips (a) Simulation (red line) and a sample of the measurement results of the VTC of the inverter while sweeping the input voltage from 0 to 2 V (blue line) and 2 V to 0 (green line). V_{OH} (output voltage when V_{IN} = 0 V), V_{OL} (output voltage when V_{IN} = 2 V), and V_M (switching threshold voltage at which $V_{IN} = V_{OUT}$) are defined in the plot. (b) VTC of the 12 measured samples along with the simulation results showing the repeatability of the process and the robustness of the proposed topology despite the hysteresis. (c) Switching threshold V_M (the intersection of the VTC with $V_{IN} = V_{OUT}$ curve) of the 12 different samples while sweeping the input voltage from 0 to 2 and 2 V to 0 versus the simulation result. (d) Gain−derivative of the transfer characteristics. (e) The minimum output voltage when the output level is logic 0 (V_{OL}) of the 12 different samples versus simulation and ideal case. (f) The maximum output voltage when the output level is logic 1 (V_{OH}) of the 12 different samples versus simulation and ideal case.

triggered register). Figure 8 shows the simulations and measurement results of 12 instances of the inverter from 4 different chips using topology (A) showing the repeatability of the rail-to-rail operation and relatively high gain. Figure 8a depicts the simulation results of the inverter voltage transfer characteristics along with the measurement result of one of samples while sweeping the input voltage in both ascending (0−2 V) and descending fashions (2−0 V). The designed inverter functions correctly and maintains adequate noise margin despite the observed shift in the switching threshold voltage of the inverter during the measurements while sweeping the voltage in both directions. Figure 8b shows the measurements results of 12 instances of the inverter from 4 different chips illustrating the repeatability of the fabrication process and the robustness of the proposed topology despite the hysteresis. The switching threshold voltages V_M (defined in Figure 8a) of the 12 inverter instances for both voltage ascending and descending sweep are plotted in Figure 8c. The inverters shows 0.24 V hysteresis voltage shift in average. All the measured circuits maintain high gain and an almost rail-to-rail output swing as shown in Figure 8d−f. More work is needed to increase the uniformity and reduce the hysteresis of the devices. Figure 9 depicts the schematic, micrograph, and the measurement results, showing correct functionality of the fabricated AND, OR, XNOR gates as well as the latch and the positive edge-triggered register. The latch is designed using two cross-coupled inverters and pass transistors. It is in hold mode when CLK is high and transparent when the CLK is low. The positive edge-triggered register is designed using two latches in master-slave configuration. When the clock is low, the master (connected to the input) is transparent while the slave is in hold mode. When the CLK turns high, the master is in hold mode while the slave latch is transparent. Thus, the output of the edge-triggered register will capture the input value at the positive edge of the CLK. The measurement results of the designed circuits fit well with the simulation, indicating the great promise of our technology and CAD flow for realizing large-scale complex MoS_2 systems. The complex four-stage integrated circuits evidence the robustness and scalability of our technology. The logic gates shown in this work form the base to a standard cell library for the synthesis of complex digital circuits (such as microprocessor for flexible wearable medical devices) using hardware description languages.[22]

A switched capacitor DC-DC converter with gain-setting of 1 is also implemented using the CAD flow. The converter consists of two FETs and a charge transfer capacitor, C_{fly} as shown in Figure 10a. Equation 4 shows V_{out} as a function of (V_{in}, I_{out}, f_{sw}) where I_{out} is the output current and f_{sw} is the converter switching frequency

$$V_{out} = V_{in} - \frac{I_{out}}{C_{fly} f_{sw}} \quad (4)$$

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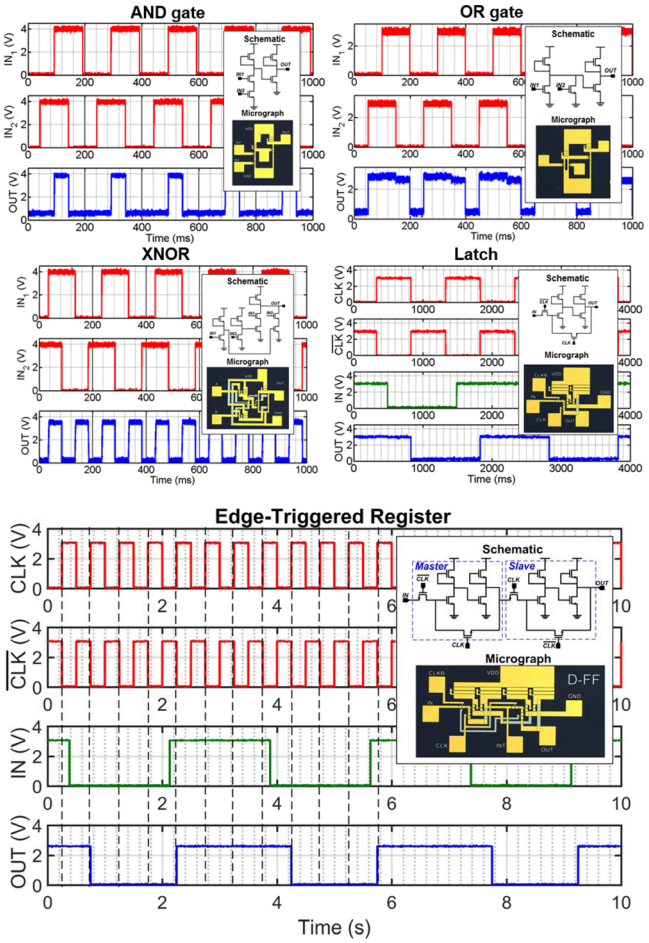

Figure 9. Schematic, micrograph, and measurement results of the fabricated AND, OR, XNOR gates, latch, and positive edge-triggered register.

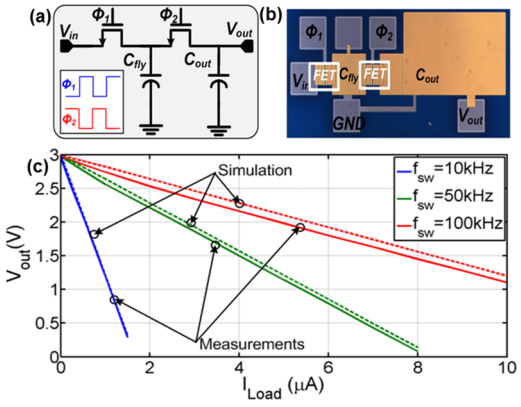

Figure 10. (a) Schematic, (b) micrograph, and (c) measurement results of the fabricated switched capacitor dc−dc converter.

In this implementation, C_{fly} is 56 pF, and the W/L of each FET is 40 μm/2 μm. Figure 10b shows the micrograph of the fabricated converter. The gates of the switches are driven externally with control signals of 0−5 V swing that are 180° out-of-phase as shown in Figure 10a, while the input is kept at 3 V. The measurement of the output voltage at different load current and switching frequency matches well with the simulation as shown in Figure 10c. The switched capacitor converter along with the digital control logic can be used for on-chip voltage regulation for dynamic voltage scaling.

The flexibility and the low-temperature process for MoS_2 electronics has a great potential for realizing ubiquitous computing systems. In this paper, we combined E-Mode FETs based on CVD MoS_2 with a computer aided design flow to realize this vision. The E-Mode device using CVD grown large area MoS_2 is realized by a gate-first process, where all the components are built and optimized before transferring the atomically thin layer of MoS_2. The statistical distribution of threshold voltage, mobility and subthreshold swing of E-mode MoS_2 confirm the high uniformity and high yield of this new technology. We developed compact virtual source models to predict the device performance using industry-standard IC design environment. We also created a custom technology library and parametrized layout cells for the transistors in industry to facilitate the mask generation for circuit fabrication. Multistage combinational and sequential circuits (NAND, NOR, XNOR, AND, OR, latch, edge-triggered register) and switched capacitor dc−dc converters are built using our flow and all show correct functionality. Our device technology, modeling, and design flow provides a platform for the co-optimization of the fabrication process and circuit performance, which allows the designers to realize the full potential of such emerging technology.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.6b02739.

Additional details about CVD growth of MoS_2, energy band diagram of MoS_2 device, MoS_2 device compact modeling, parametric layout cell (PDF)

■ AUTHOR INFORMATION

Corresponding Authors

*(L.Y.) E-mail: liliyu@mit.edu. Fax: +1 (617) 258-7393).
*(D.E.-D.) E-mail: deldamak@mit.edu. Tel: +1 (617) 955-9645.

Author Contributions

D.E.-D. and L.Y. contributed equally to this work.

Notes

The authors declare no competing financial interest.

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