MoS_2 FET Fabrication and Modeling for Large-Scale Flexible Electronics

Lili Yu, Dina El-Damak, Sungjae Ha, Shaloo Rakheja, Xi Ling, Jing Kong,
Dimitri Antoniadis, Anantha Chandrakasan, Tomás Palacios
Massachusetts Institute of Technology, Cambridge, MA 02139, U.S.A.
Tel: +1 (617) 460-7364, Fax: +1 (617) 258-7393, Email: liliyu@mit.edu, deldamak@mit.edu

Abstract

We present a state-of-the-art fabrication technology and physics-based model for molybdenum disulfide (MoS_2) field effect transistors (FETs) to realize large-scale circuits. Uniform and large area chemical vapor deposition (CVD) growth of monolayer MoS_2 was achieved by using perylene-3,4,9, 10-tetracarboxylic acid tetrapotassium salt (PTAS) seeding. Then, a gate first process results in enhancement mode FETs and also reduces performance variation and enables better process control. In addition, a Verilog-A compact model precisely predicts the performance of the fabricated MoS_2 FETs and eases the large-scale integrated design. By using this technology, a switched capacitor DC-DC converter is implemented, and the measurement of the converter shows good agreement with the simulations.

Keywords: MoS_2, 2D materials, large scale, flexible IC.

Introduction

MoS_2 has gained great interest for its atomic planar nature and mechanical flexibility to realize lightweight and flexible electronic systems on arbitrary surfaces. It has higher carrier mobility compared to amorphous Si and organic semiconductors and its 1.8eV bandgap allows high on-off ratio to construct low-cost flat-panel driving circuits [1]. Despite of its promising characteristics, applications up to date have been limited to single or a few devices scale system. The challenges in large-scale system design with a newly-introduced material mainly remain in three issues: material growth and transfer, device integration, and circuit simulations. First, a growth technology for large-area homogeneous monolayer MoS_2 with large domain size and a low doping clean transfer is required. Second, enhancement mode FETs, with positive and reproducible threshold voltage (V_T), are necessary to cascade logic circuits and complete a stand-alone system. For CVD MoS_2, only depletion mode FETs [1,2] have been reported, which require external bias to drive other logic gates. Positive V_T is hard to achieve due to the sensitivity of MoS_2 to doping and the difficulty for dielectric integration. Lastly, earlier technologies lack computer-aided design tools to facilitate the design of complex systems. In this paper, we address all these issues by using PTAS promoted CVD MoS_2 growth, gate-first fabrication process and Verilog-A compact model for circuit simulation.

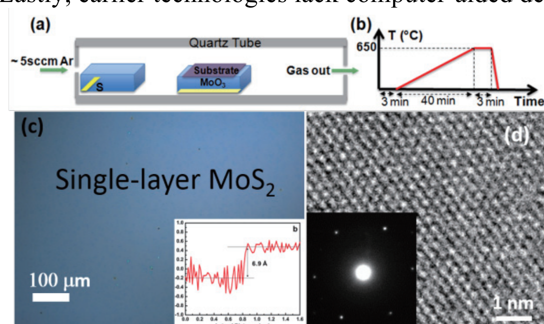

Fig. 1 (a) A schematic illustration of the MoS_2 CVD system. (b) The temperature programming process used for a typical growth. (c) Optical micrographs and thickness profile (inset) of monolayer MoS_2. (d) HRTEM image and the corresponding selected area electron diffraction (SAED) pattern (inset) show the hexagonal crystal nature and the high quality lattice structure of MoS_2.

Material Growth

Fig. 1(a) shows the experimental setup for the CVD synthesis of monolayer MoS_2, using S and MoO_3 as the precursor, and PTAS as the seeding promoter. The furnace temperature profile during growth is shown in Fig. 1(b). An optical image of as-grown CVD MoS_2 is shown in Fig. 1(c), demonstrating a good uniformity and a high coverage approaching 100%. The domain size of this sample is 30 µm on average. The thickness is measured as 6.9 Å, a typical monolayer MoS_2 thickness, using atomic force microscopy (Fig. 1(c), inset). The high quality of CVD-grown MoS_2 is also evidenced by the highly ordered lattice structure observed under high resolution TEM as well as the crystal structure from diffraction pattern (Fig. 1(d)).

Device Fabrication

Next, device fabrication (Fig. 2) starts with gate patterning by photolithography and 5nm Cr/30 nm Au/30nm Pd metal stack deposition on a SiO_2 substrate. 20 nm Al_2O_3 is then deposited using atomic layer deposition and annealed in forming gas for 30 minutes at 450°C to remove the fixed charge inside the dielectric. Via hole is patterned, followed by etching using reactive ion etching by Cl_2/BCl_3 plasma. Then, as-grown MoS_2 CVD sample is coated with PMMA and soaked in hot KOH solution at 85°C. The SiO_2 layer is etched away and MoS_2/PMMA stack is released then transferred to a new target substrate, followed by annealing process to clean the polymer residue. O_2 plasma is then used to isolate MoS_2 channel. Ohmic contacts and measurement pads of the devices/circuits are formed by depositing a 90 nm Au layer or 5nm Ti/90nm Au metal stack. Fig. 3 shows a top view of a test chip with different device components as well as circuits.

For conventional MoS_2 FETs, with gate-last process, dielectric integration is usually conducted at low temperature or assisted by seeding layer, both resulting in fixed charge and trapped states inside the dielectric or at the interface. This causes extra scattering hence degradation of mobility as well as shift in V_T. Using the gate-first process instead, the critical components are fabricated before the MoS_2 transfer step, achieving high gate dielectric and interface quality and the

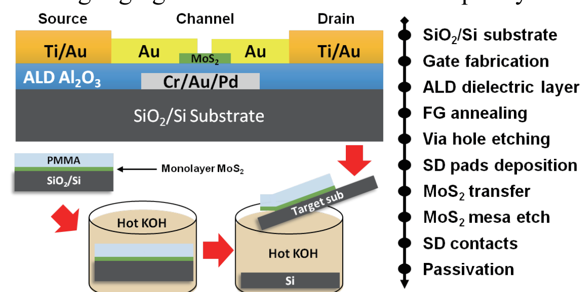

Fig. 2 Fabrication technology for large scale MoS_2 electronics.

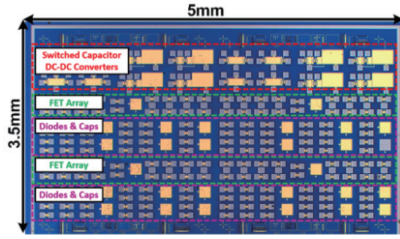

Fig. 3 Optical micrograph of the test chip fabricated using CVD grown monolayer MoS_2, showing arrays of FETs, diodes and switched capacitor DC-DC converters

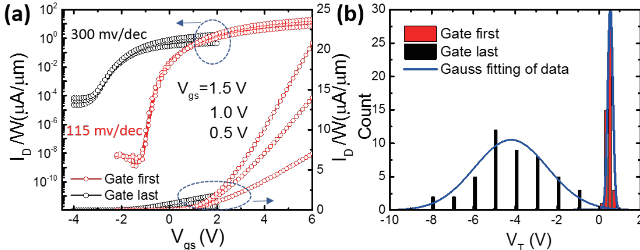

Fig. 4 (a) Transfer characteristics in linear (right y-axis) and log scale (left y-axis) and (b) Statistics of V_T of MoS_2 FETs (channel length of 2um) from different fabrication technologies.

potential for low effective oxide thickness scaling. MoS_2 FETs with gate-first technology show larger V_T, 10x larger on current, 100x smaller off current and steeper subthreshold slope (Fig. 4(a)) in comparison with gate-last based FETs. Devices from gate-first process have average V_T of 0.54V with standard deviation of 0.12 V while those from gate-last process have average V_T of -4.20 V and standard deviation of 1.75 V (Fig. 4(b)).

Computer-Aided Design Flow for MoS_2 Technology

A complete computer-aided design (CAD) flow with device modeling, circuit simulation and parametric cell-based layout is developed in order to improve the design process of complex systems as shown in Fig. 5.

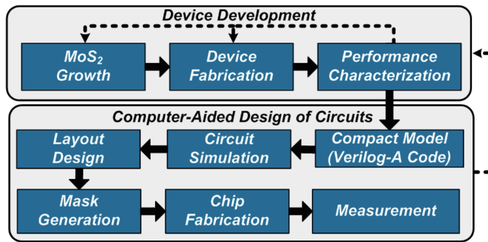

Fig. 5 Flow for large-scale MoS_2 integrated circuit development.

First, a drift diffusion Verilog-A compact (DDC) model is derived for the MoS_2 transistors. The model describes I-V characteristics of an FET, based on the electron transport properties of atomically thin MoS_2 substrates [3]. Given that the current in a FET is simplified as

$$I_D = \frac{1}{2} W (Q_{is} + Q_{id}) f(v_{sat}) v_{sat}, \qquad (1)$$

where W is the device width, Q_{is} and Q_{id} are the channel charges at source and drain, respectively, and v_{sat} is the saturation velocity of carrier. The $f(v_{sat})$ is given by

$$f(v_{sat}) = \frac{(Q_{is}-Q_{id})/C_{invi}V_{DSAT}}{(1+((Q_{is}-Q_{id})/C_{invi}V_{DSAT})^{\beta})^{1/\beta}}, \qquad (2)$$

where C_{invi} is the channel-to-gate capacitance, and β is an empirical parameter that can be obtained from experimental data. Fig. 6 depicts the modeled I-V characteristics with the measurement data from a MoS_2 FET.

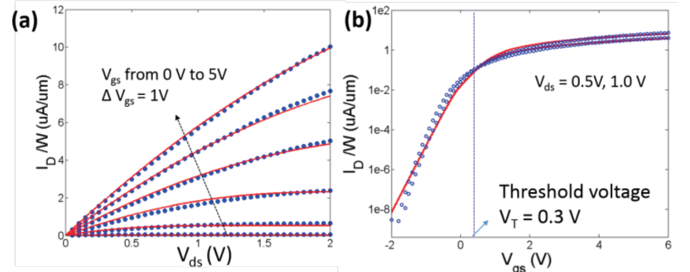

Fig. 6 I-V curves of a MoS_2 FET from DDC model (line) and measurement (dots).

With the parameters extracted from FETs, the DDC model is implemented in Verilog-A language to enable circuit simulation as in standard silicon ASIC design process. Lastly, the FET layout is implemented in a parametric cell to ease the layout of large-scale system designs.

Switched Capacitor DC-DC Converter

A switched capacitor DC-DC converter is implemented using the CAD flow. The converter consists of two MoS_2 switches and a charge transfer capacitor, C_{fly} as shown in Fig. 7(a). As shown in Eq. (3), the output voltage of the converter, V_{out}, is a function of V_{in}, I_{out} and f_{sw} where I_{out} is the output current and f_{sw} is the converter switching frequency [4].

$$V_{out} = V_{in} - \frac{I_{out}}{C_{fly} f_{sw}} \qquad (3)$$

In this implementation, C_{fly} is 56pF, and the switch size is 40μm/2μm. Fig. 7(b) shows the micrograph of the fabricated converter. The gates of the switches are driven externally with 0-5V swing control signals that are 180° out-of-phase as shown in Fig. 7(a), while the input is kept 3V. The measurement of the output voltage while varying load current and switching frequency matches well with the simulation as shown in Fig. 8.

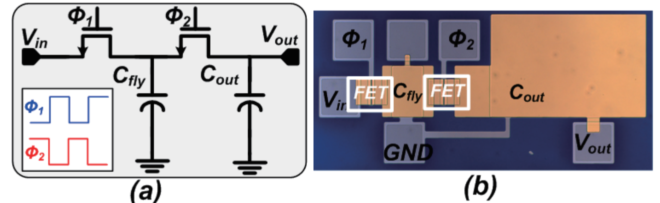

Fig. 7 (a) Schematic diagram of the switched capacitor converter and (b) micrograph of the fabricated converter.

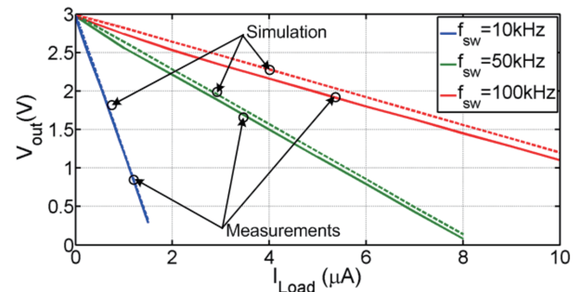

Fig. 8 Simulation (dotted) and measurements (solid) of the output voltage versus the load current of MoS_2 SC DC-DC converter.

Acknowledgments

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