

High-Performance WSe₂ Complementary Metal Oxide Semiconductor Technology and Integrated Circuits

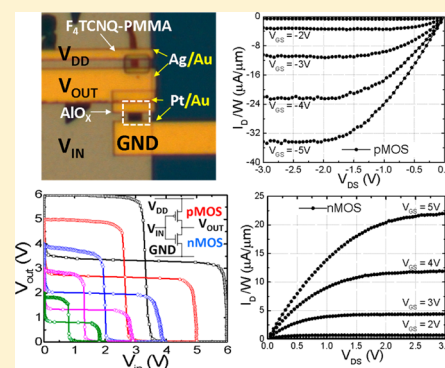
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ABSTRACT: Because of their extraordinary structural and electrical properties, two-dimensional materials are currently being pursued for applications such as thin-film transistors and integrated circuit. One of the main challenges that still needs to be overcome for these applications is the fabrication of air-stable transistors with industry-compatible complementary metal oxide semiconductor (CMOS) technology. In this work, we experimentally demonstrate a novel high performance air-stable WSe₂ CMOS technology with almost ideal voltage transfer characteristic, full logic swing and high noise margin with different supply voltages. More importantly, the inverter shows large voltage gain (~ 38) and small static power (picowatts), paving the way for low power electronic system in 2D materials.

KEYWORDS: Transition metal dichalcogenides, integrated circuits, complementary logic, CMOS electronics, air stable doping, low power electronics



Two-dimensional (2D) crystals, including graphene, hexagonal boron nitride, and transition metal dichalcogenides (TMD), have outstanding properties for developing the next generation of electronic devices.^{1–7} Their extreme thinness, down to a single layer, allows almost perfect electrostatic control of the transistor channel, making them robust to short channel effects and ideal for low power applications.⁸ In addition, these materials offer excellent mechanical flexibility, optical transparency, and favorable transport properties for realizing electronic, sensing, and optical systems on arbitrary surfaces.^{9–12} These thin, lightweight, bendable, highly rugged, and low-power devices could bring dramatic changes to information processing, communications, and human-electronic interaction. One of the main challenges that still needs to be overcome for these applications is the fabrication of air-stable transistors with industry-compatible complementary metal oxide semiconductor (CMOS) technology.^{13,14} CMOS logic has high noise immunity, well-established circuit designs, low static power consumption, and high density of integration.¹⁵

CMOS is made from complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) with matched threshold voltage and current level. CMOS logic circuits on two-dimensional (2D) materials have first been demonstrated on structures with two different layered materials, where one material is used for the n-type MOSFET (nMOS) device and a different material system is used for the p-type MOSFET (pMOS).^{16,17} Logic inverters

have been fabricated with this heterogeneous combination, however these logic gates showed small gain (less than 2) and unmatched input output voltage, leading to zero noise margin.^{16,17} To achieve a single-2D-material CMOS technology, WSe₂ is arguably a more promising semiconductor than the more explored MoS₂ because of the more balanced conduction and valence band edges to different work functions metals and symmetric electron and hole effective mass. An integrated WSe₂ CMOS technology has been demonstrated using gas-phase doping.¹³ The device shows however short lifetime in air, and the absence of rail-to-rail performance indicates significant static leakage current between the supply line and ground, which leads to large power consumption. More recently, an electrostatically doped WSe₂ CMOS technology has been reported, however extra terminals and multiple voltage bias supplies are needed, which significantly increases the circuit complexity.¹⁴ Hence, to the best of our knowledge there is still no report of an integrated 2D CMOS technology that is stable and offers high-enough noise margin for actual applications.

In this Letter, we experimentally demonstrate an air-stable novel high performance WSe₂ CMOS technology with excellent voltage transfer characteristic, full logic swing and high noise margin. More importantly, the inverter shows high

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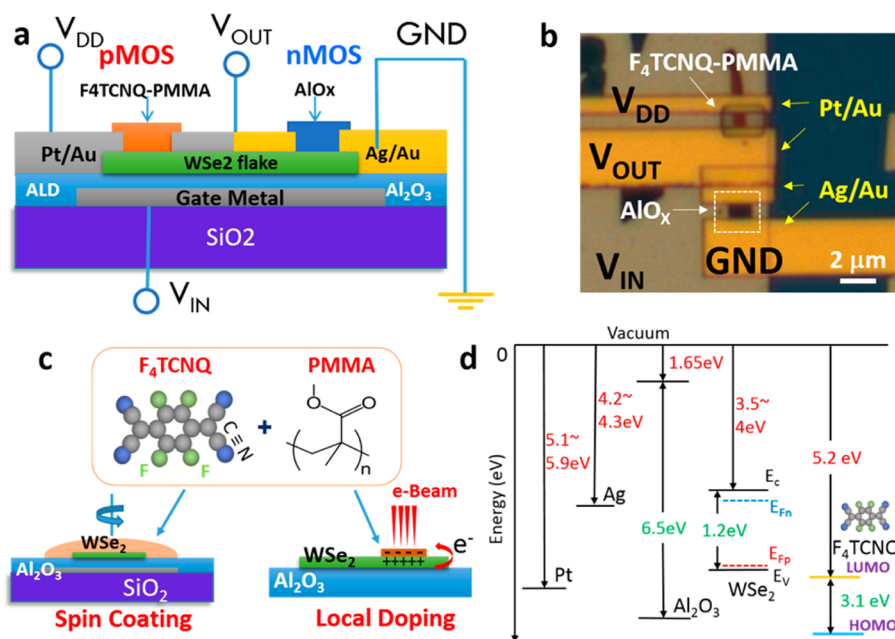


Figure 1. Structure, doping method, and band alignment. (a) Schematic and (b) optical image of device structure of WSe₂ CMOS technology with F₄TCNQ-PMMA doped pMOS and AlO_x encapsulated nMOS. The source electrode of the nMOS and pMOS transistors are connected to ground and V_{dd} power supply, respectively. Their gates are connected with each other as the input node while the drains are connected to serve as the output node. (c) Localized and air-stable p type doping method for WSe₂ using F₄TCNQ-PMMA mixture. (d) Band diagram in the CMOS system.

voltage gain and static power consumption as low as pico-watts, paving the way for ultralow power system in 2D materials.

Figure 1a shows the schematic of the device structure used in this work. nMOS and pMOS transistors are monolithically integrated on a single WSe₂ flake. The device fabrication starts with gate patterning and 5 nm Cr/30 nm Au/30 nm Pd metal stacks deposition on a SiO₂ substrate. Then 20 nm Al₂O₃ is deposited using atomic layer deposition (ALD) on the gate electrode. A 30 min forming gas annealing at 450 °C is then applied to remove the fixed charge inside the dielectric. The thin ALD dielectric layer provides good electrostatic control of the gate, and matched voltages of source/drain and gate. Atomically thin WSe₂ flakes are achieved via micromechanical exfoliation and then transferred on to the gate stack (see Methods section), followed by high-temperature annealing to clean the polymer residue. Then a low work function metal (i.e., Ag) and a high work function metal (i.e., Pt) are used to contact the nMOS and pMOS FETs (Figure 1c), respectively. The nMOS is then covered with AlO_x before p-doping (see Methods section for details). To improve the pMOS performance, tetrafluoro-tetracyanoquinodimethane (F₄TCNQ)^{18,19} is used to dope the WSe₂ channel, which helps to reduce the pMOS Schottky barrier width and also to increase the tunneling hole current. To increase the long-term stability of F₄TCNQ, we incorporated it into a F₄TCNQ-Poly(methyl methacrylate) (PMMA) mixture by using Anisole as a solvent (Figure 1c) with different weight ratio of F₄TCNQ. The solution is spin-coated on the sample and the F₄TCNQ molecules are trapped in the PMMA polymer chain network. Then electron beam lithography is used to expose the F₄TCNQ-PMMA mixture where the nMOS devices will be located, following by development using MIBK/IPA developer to remove the F₄TCNQ-PMMA mixture in those regions. As a result, the doping is localized only in pMOS where F₄TCNQ-PMMA left. Charge transfer happens between the F₄TCNQ-PMMA layer and the WSe₂ underneath it, achieving localized p-

type doping. Figure 1b is the optical image of the final integrated CMOS inverter on WSe₂ flake. Figure 1d shows the work function alignment of contact metal (Ag, Pt), oxide (Al₂O₃), semiconductor band diagram (WSe₂) and acceptor molecule energy level (F₄TCNQ) in this CMOS technology. The highest occupied molecular orbital energy of F₄TCNQ is lower than the valence band edge of WSe₂, which induces the transfer of electrons from WSe₂ to F₄TCNQ, resulting p doping in WSe₂, which will be discussed in detail later. High/low work function metals are deliberately chosen to help the charge injection of hole and electron, respectively. It should be noted that the maximum current of the nMOS devices does not show any change after process steps of AlO_x deposition, F₄TCNQ-PMMA coating, writing, and development.

The transfer characteristics of WSe₂ nMOS transistors with a Ag/Au metal stack contact on an Al₂O₃ substrate are shown with a black line in Figure 2a. There is a highly conductive electron current and suppressed hole current, with high on-off ratio close to 10⁸. In our experiment, WSe₂ flakes exfoliated on top of SiO₂ usually show ambipolar performance with slightly higher hole branch current (inset, Figure 1a), while flakes on Al₂O₃ substrate (such in our devices, where Al₂O₃ is used as gate dielectric) without forming gas annealing show degenerate electron doping (red dashed line in Figure 1a). The doping comes from the fixed charge on the surface or in the bulk of the dielectric layer or interaction between the 2D material and the substrate, which has been previously observed in both graphene^{20,21} and MoS₂²² on different substrates. The positive fixed charge causes charged impurity scattering in WSe₂, which degrades mobility and makes it difficult to turn off the device. Thus, high-temperature annealing is needed to improve the dielectric quality without degrading material quality as well as to tune the nMOS threshold voltage. In order not to damage the WSe₂ layer during the high-temperature annealing, we developed a gate metal/dielectric stack-first fabrication process,

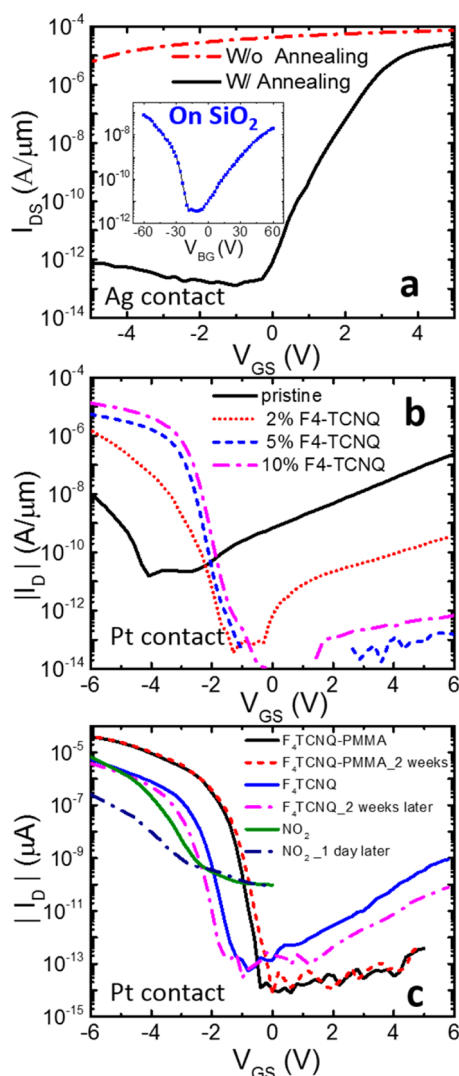


Figure 2. Effect of contact metals and dopants. (a) Transfer characteristics of Ag-contacted WSe₂ FET on Al₂O₃ substrate with (black solid line) and without (red dashed line) gas annealing treatment. Inset, Ag-contacted WSe₂ FET on SiO₂ substrate. Fixed charge in the dielectric layer has an important doping effect. (b) Transfer characteristics of Pt-contacted WSe₂ FET with different concentration of F₄TCNQ. When F₄TCNQ concentration in PMMA increases, the hole current increases while the electron density significantly decreases. (c) Long-term stability of pMOS fabricated by three different doping methods. Device doped by 10% F₄TCNQ/PMMA mixture shows almost no current change after 2 weeks; device doped by 2% F₄TCNQ/IPA solution shows 30% current decrease after 2 weeks, while device doped by NO₂ gas shows 20 times current reduction after only 1 day.

which allows the transfer of the WSe₂ layer after the gate dielectric has been annealed at high temperature.

The transfer characteristics of pMOS WSe₂ transistors with a Pt ohmic contact technology on an Al₂O₃ substrate are shown in Figure 2b (red dash-dot line). Opposite to the Ag/Au contacted nMOS device, this device exhibits ambipolar performance with low electron and hole current. To increase the hole-based current, F₄TCNQ is used to dope the channel. This molecule has been reported to be an effective p-type dopant in single-wall carbon nanotubes field effect transistors¹⁹ as well as organic semiconductors such as zinc-phthalocyanine (ZnPc).²³ The transfer characteristics of WSe₂ FETs

doped by different concentration of F₄TCNQ/PMMA solution are shown in Figure 2b. The hole current of the device increases, the electron current decreases, and the threshold voltage also decreases as the F₄TCNQ concentration increases. With 10% F₄TCNQ in PMMA, the hole current increases by more than 1000× while the electron current decrease more than 6 orders of magnitude than that of devices before doping.

The long-term stability of the new F₄TCNQ/PMMA localized doping was also studied and compared with other p-doping methods, as shown in Figure 2c. After 2 weeks exposure to air, the on-state hole current does not change while the current increases slightly in the subthreshold region. These results are significantly more stable than with other doping methods traditionally used in the literature, for example, exposure to strong oxidizing NO₂ gas²⁴ or directly coating with F₄TCNQ/IPA solution (see Methods section for details). For the NO₂ gas doping, the hole current drops by more than 20 times in the first 24 h, while for pure F₄TCNQ (2% in IPA) doping, the current decreases by 30% after 2 weeks. F₄TCNQ has been found to be unstable and volatile, especially at elevated temperature,²⁵ because of its diffusion properties, thus PMMA scaffold effectively stabilize F₄TCNQ on WSe₂ surface.

After optimizing the substrate, metal contacts, and dopants, we achieve simultaneously high-performance nMOS and pMOS FETs, whose transport performance are shown in Figure 3. The WSe₂ flake has a thickness of 5 nm and the nMOS/pMOS transistors have a channel length of 1 μm . From the transfer characteristics, they are both enhancement mode transistors with high on/off ratio (10^7 for nMOS and 10^8 for pMOS). The threshold voltage for the nMOS and pMOS devices are 2 and -1.8 V, respectively, while the subthreshold swings are 167 and 162 mV/dec. The devices show a linear current behavior at low drain bias voltages and excellent current saturation at higher drain biases with on-state current density of 22 and 35 $\mu\text{A}/\mu\text{m}$ in nMOS and pMOS transistors, respectively. The conservative estimation (including contact resistance) of mobility for electrons and holes are 27.4 and 42.6 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, respectively. In a field effect transistor, the effective channel length is shortened with increasing in drain bias beyond saturation. This phenomena, known as channel length modulation, is typically characterized through the parameter λ in the drain current expression (nMOS as an example) $I_D = [(uC_{ox}W)/(2L)][(V_{GS} - V_{TN})^2(1 + \lambda V_{DS})]$, where μ is the carrier mobility, C_{ox} is the gate capacitance, W and L are the device width and length, V_{GS}/V_{DS} is the gate/drain voltage, and V_{TN} is the threshold voltage of nMOS, respectively. From Figure 3b,d, both the nMOS and the pMOS transistors have very small channel length modulation. Therefore, the output resistance $r_o = (\partial I_D / \partial V_{DS})^{-1} = (\lambda I_D)^{-1}$ is large. This is very important to achieve high gain in inverter or amplifier, which is proportional to r_o .

The nMOS and pMOS technologies described above were used to fabricate an integrated CMOS logic inverter (Figure 1a). The voltage transfer characteristics (VTC) of the fabricated CMOS inverter are shown in Figure 4a. The WSe₂ CMOS inverter shows excellent inverting performance under a wide range of V_{dd} values, 2 to 6 V, which gives full logic swing, abrupt transition, symmetrical shape and high noise margin. In addition, there is almost zero current under static conditions (Figure 4a, inset). The sharp transition between the two logic states can be characterized by the voltage gain $A_v = dV_{out}/dV_{in}$ (Figure 4b). As shown in Figure 4b, the gain is close to zero, except at the transition region where the gain experiences a

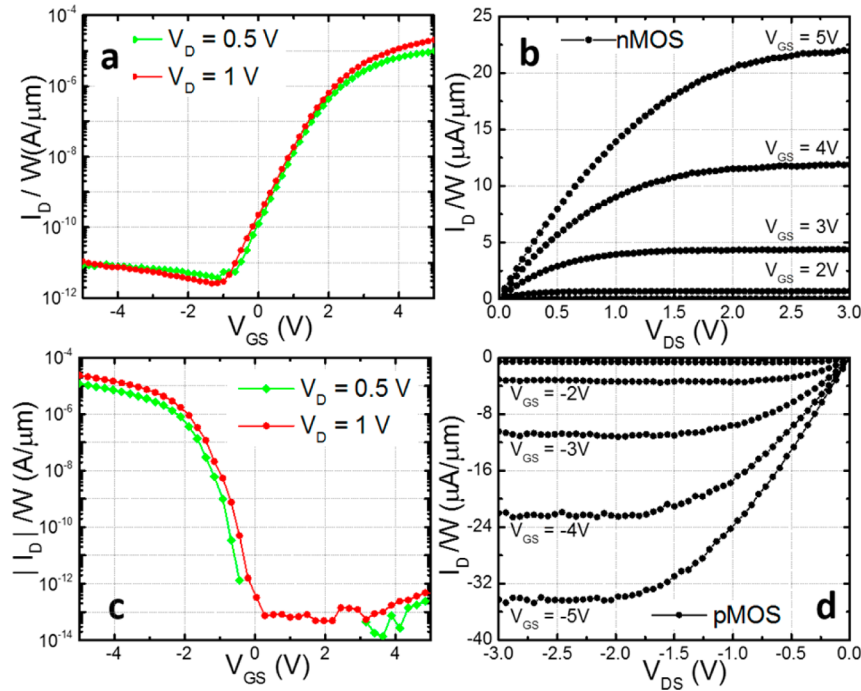


Figure 3. Transfer and output characteristics of transistors. WSe₂ nMOS (a) transfer characteristics and (b) output characteristics; WSe₂ pMOS (c) transfer characteristics and (d) output characteristics. Both transistors show high on–off ratio, high on current density, and excellent current saturation.

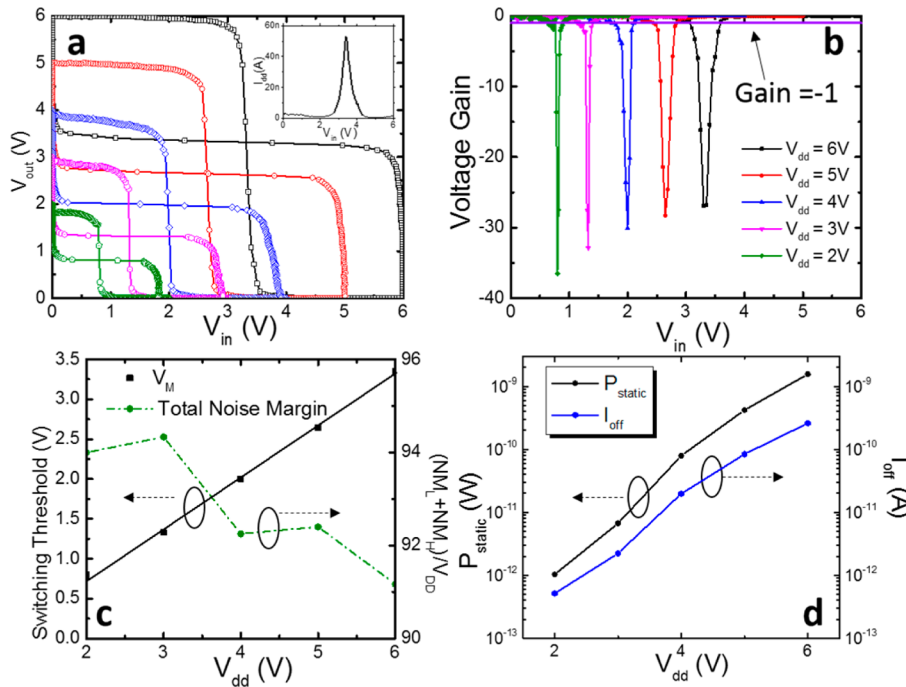


Figure 4. Integrated circuit characteristics. (a) VTC and corresponding butterfly curves of WSe₂ CMOS logic inverter with V_{dd} supply from 2 to 6 V. Inset: current change with input voltage. (b) Voltage gain of WSe₂ CMOS logic inverter, gain equaling to -1 is denoted by the purple line, the peak gain decrease with the increase of V_{dd} value. (c) Switching threshold (left axis) and ratio of total noise margin (right axis) to V_{dd} as a function of V_{dd} . (d) Static power consumption (left axis) and off current (right axis) of the CMOS inverter as a function of V_{dd} .

sharp peak at half V_{dd} voltage, with a maximum value of 38 for $V_{dd} = 2$ V. A gain larger than 1 is important for cascade logic application because it makes the circuit regenerative and robust to errors, which is very important for multistage logic applications. When V_{dd} decreases, the peak gain increases and the transition region becomes narrower. From a small signal

model of an inverter, the voltage gain can be calculated using $A = (g_{mn} + g_{mp})(r_{op} || r_{on}) = [(\lambda_n + \lambda_p)(V_g - V_{Tn})]^{-1} \propto (V_{dd}/2 - V_{Tn})^{-1}$, thus the gain decreases with increasing V_{dd} . In previous work,¹³ researchers showed the opposite trend, which may indicate that the device performance is unstable with significant current leakage between the power supply and ground, which

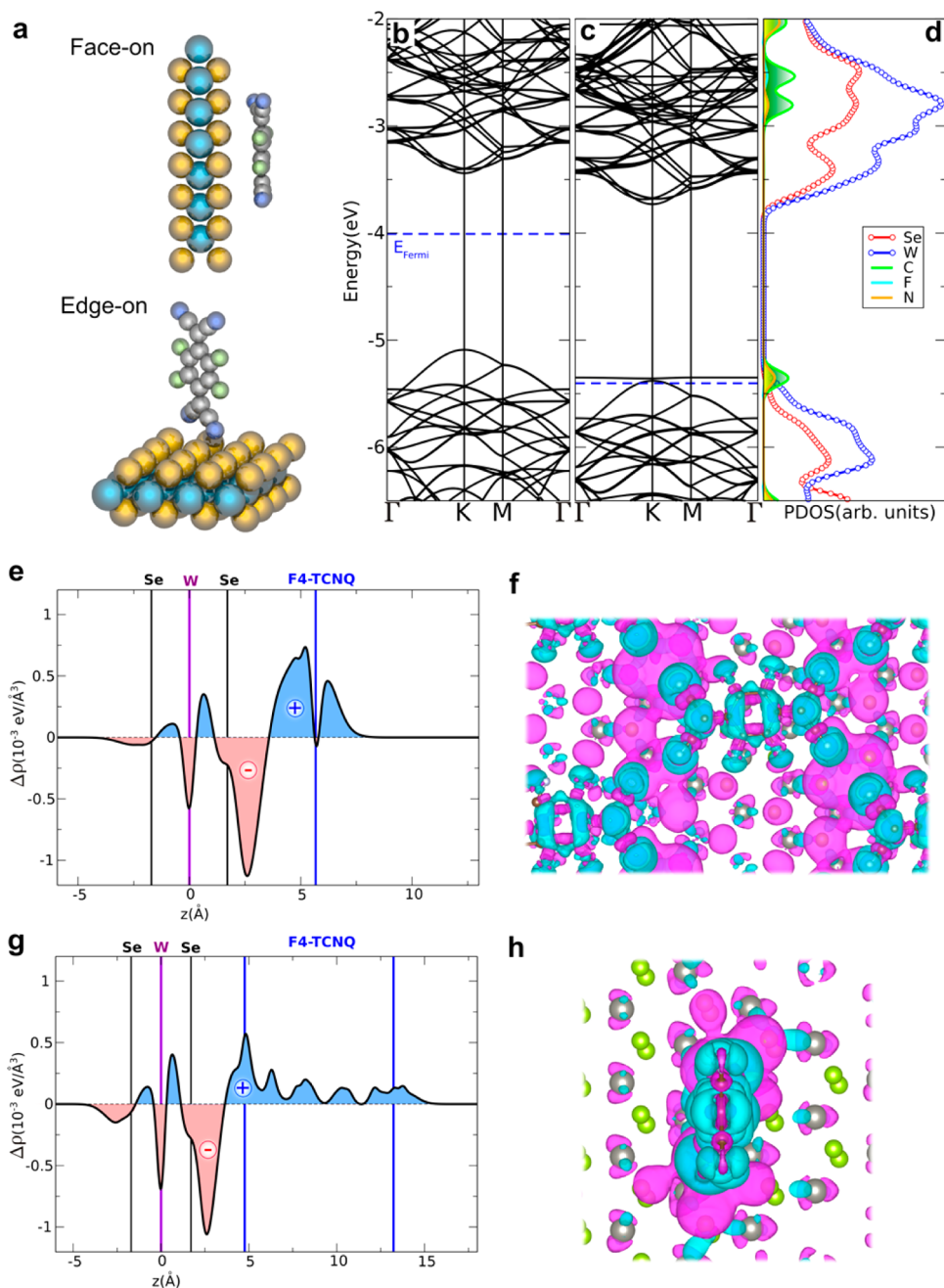


Figure 5. First principle calculations. P-type behavior induced by F₄-TCNQ on WSe₂ layers. (a) Molecular structures of F₄-TCNQ on top of WSe₂ at face-on and edge-on geometries. (b,c) Calculated band structure of pristine WSe₂ and face-on interface, respectively. (d) Projected density of states (PDOS) on different atoms of the system at face-on geometry on the valence states used in the calculation for each specie. (e,g) Plane-averaged electron density difference along the direction perpendicular to the interface of face-on and edge-on structural configurations, respectively. The blue and red colors indicate electron accumulation and depletion. (f,h) Top views of the charge density differences between F₄-TCNQ and WSe₂ systems at face-on and edge-on interfaces, respectively. The iso-surfaces are at $1.4 \times 10^{-3} e/\text{\AA}^3$. Red means charge depletion and blue is charge accumulation.

prevents the static output voltage from reaching the supply voltage. The stable doping technology adopted in this paper makes the device scale properly with V_{dd} , offering a wide range of operating biasing conditions to match the power requirements of each particular application.

The switching threshold (SW, the voltage at which the output voltage is the same as the input voltage) and noise margin are important parameters for device robustness. SWs for our WSe₂ inverter are plotted as a function of V_{dd} in Figure 4c. It is linear with V_{dd} with a slope close to 0.5. The total noise

margin of the inverter is higher than 90% of V_{dd} , which shows the large tolerance of the device to intrinsic or extrinsic noise. This large noise margin, together with matched input–output, high gain, makes our devices easy to be integrated into multistage large system.

Finally, the biggest advantage of CMOS technology is the power consumption. The power is typically divided in dynamic and static power. Static power can be expressed as $P_{static} = V_{dd}(I_{static_low} + I_{static_high})/2$ at static state ($V_{in} = 0$ V or $V_{in} = V_{dd}$) while the dynamic power is proportional to V_{dd}^2 and will

not be discussed here. The static current and the power consumption, averaged at high and low state, under different V_{dd} values for our integrated logic inverter are plotted in Figure 4d. The current increases with V_{dd} exponentially, because of the tunneling nature of leakage current under static operation. The static power consumption reaches 2 pW when V_{dd} is 2 V. This is at least orders of magnitude lower than previous work¹³ where the static power is roughly estimated to be in the hundred nanowatts range for V_{dd} of 3 V. This demonstrates the high potential of WSe₂ CMOS technology for ultralow power electronics.

To further understand the doping effect of F₄TCNQ on WSe₂, we performed first-principles calculations using density functional theory, including van der Waals interactions (see Methods section for further details). We considered supercells composed of F₄TCNQ molecules at two different molecular configurations as shown in Figure 5a. It was found that the configurations where F₄TCNQ molecules lie down on WSe₂ layers (face-on) bind stronger than those where the molecules assume a tilted orientation (edge-on). The energy difference is as large as 0.11 eV per F₄TCNQ molecule that points to a potential preferential orientation at the interface. Even though the binding energies are different, the electronic structure of both geometries shows similar features. The calculated band structures, including van der Waals dispersion forces of WSe₂ layers before and after the doping at face-on geometry are shown in Figure 5a,b, respectively. Similar results are obtained for edge-on geometry (not shown). The adsorption of F₄TCNQ induces the appearance of extra-hole energy levels near the top of the valence band of WSe₂, mainly composed by s and p states from C atoms at the molecule, with smaller contribution from N (Figure 5d). A charge transfer of 0.25 electrons per unit cell is observed from WSe₂ to F₄TCNQ, which induces a shift to lower energies of the Fermi level (Figure 5b). This explains the F₄TCNQ p-type doping behavior in WSe₂, which remarkably agrees with the experimental measurements discussed above. The charge transfer between WSe₂ and F₄TCNQ also creates an interfacial dipole moment of 2.94 and 7.02 D at face-on and edge-on configurations, respectively. This is observed mainly at the first Se-layer closer to the F₄TCNQ molecules (Figure 5e,g). The charge density differences for face-on (Figure 5f) and edge-on (Figure 5h) interfaces point to a higher charge depletion at the WSe₂ layer between the F₄TCNQ molecules and at the N atoms, where the molecules stand up. These results strongly suggest that F₄TCNQ on top of WSe₂ can be used as an effective p-type dopant in WSe₂.

In conclusion, we report a high-performance CMOS technology in WSe₂. We systematically study the effect of metal contact, the substrate and the acceptor doping to the performance of WSe₂ devices. High on–off ratio, high current density, and excellent current saturation are achieved in both nMOS and pMOS transistors. By fabricating CMOS inverters, we show that this technology presents excellent voltage transfer characteristic, full logic swing and high noise margin, which is stable in the air. More importantly, the inverter shows large voltage gain (~38), total noise margin larger than 90% of operating voltage, small static power (picowatts). We expect that the air-stable, noise-robust, high-gain, and low-power CMOS technology presented in this paper can be easily applied to larger circuits in the near future, thanks to the fast progress in large scale CVD WSe₂ growth.²⁶ This work therefore paves the way for ultralow power system in 2D materials.

Methods. *ALD.* The low-temperature ALD deposition of Al₂O₃ was performed on a commercial Savannah ALD system from Cambridge NanoTech at 250 °C using alternating cycles of H₂O and trimethylaluminum (TMA) as the precursors.

Dry Transfer. The WSe₂ was micromechanically exfoliated from commercially available bulk natural crystal (Nanosurf) on a previously prepared transfer slide using cleanroom grade low-tack tapes.²⁷ The transfer slide consisted of a supporting stack of transparent materials and a polymer release layer. The supporting stack was made of glass/Sylgard 184 polydimethylsiloxane (PDMS)/clear packing tape and the polymer release layer was a double layer of methyl methacrylate (MMA). Small squares of WSe₂/MMA/tape/PDMS stack were then cut out using a sharp clean blade and transferred on another clean glass slide. The glass slide and prepatterned substrate were then mounted on the in-house alignment transfer setup, consisting of an optical microscope and micromanipulator. The target flake and substrate with gate pattern were carefully aligned and engaged in contact with stage temperature of 35 °C. The stage was then heated to 130 °C and the glass slide disengaged from the target substrate. At the same time, MMA with WSe₂ flakes was released from tape/PDMS/glass stack and successfully transferred to the gate pattern. The sample was then soaked in acetone and annealed at 200 °C in Ar/H₂ to remove the polymer residue from the transfer process.

AFM. Atomic force microscopy (AFM) for identifying the thin film thickness was performed on a Veeco Dimension 3100 system.

nMOS Passivation. PMMA on top of nMOS region was exposed by electron beam lithography, followed by development. Then Al metal was deposited and exposed to air for oxidization for three times to get the desired thickness with 1.5 nm thick Al each time. Then the sample was heated on a hot plate in air for several hours at 100 °C for full oxidization.

NO₂ gas and F₄TCNQ/IPA Doping. For NO₂ gas doping, the sample was exposed to NO₂ gas for several minutes for WSe₂ to absorb NO₂ gas on its surface. For F₄TCNQ/IPA doping, F₄TCNQ was first mixed into IPA solution by weight ratio and then the solution was coated onto the WSe₂ device. Pure F₄TCNQ was left on the sample surface after IPA evaporates.

Device and Circuit Characterization. Device characterization was performed using an Agilent 4155C semiconductor parameter analyzer and a Lakeshore cryogenic probe station with micromanipulation probes. All measurements were done in vacuum (3×10^{-6} Torr) at room temperature.

First-Principles Calculations. Calculations were based on ab initio density functional theory using the SIESTA code.²⁸ The generalized gradient approximation²⁹ and nonlocal van der Waals density functional³⁰ were used together with double- ζ plus polarized basis set, norm-conserving Troullier–Martins pseudopotentials.³¹ Atomic coordinates were allowed to relax using a conjugate-gradient algorithm until all forces were smaller in magnitude than 0.01 eV/Å. Relevant lattice constants (in-plane and out-of-plane) were optimized for each system. To avoid interactions between supercell images the distance between periodic images of the F₄TCNQ/WSe₂ structures along the direction perpendicular to the WSe₂-plane was always larger than 20 Å. The resolution of the real-space grid used to calculate the Hartree and exchange-correlation contribution to the total energy was chosen to be equivalent to 150 Ry plane-wave cutoff. The number of k -points was chosen according to the Monkhorst–Pack scheme³² and was set to the equivalent of

a $45 \times 45 \times 1$ grid in the primitive unit cell of WSe_2 , which gives well converged values for all the calculated properties. We used a Fermi–Dirac distribution with an electronic temperature of $k_B T = 21$ meV.

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Author Contributions

T.P. and L.Y. conceived and supervised the research. L.Y. and A.Z. fabricated the device. L.Y. performed the measurements and data analysis. E.J.G.S. performed the van der Waals first-principles simulations. X.Z., Y.L., and Y.Z. helped with fabrication process. L.Y. and T.P. cowrote the manuscript. All authors commented on the manuscript and discussed the results.

Notes

The authors declare no competing financial interest.

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