Negative Capacitance Carbon Nanotube FETs

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***Abstract*— As continued scaling of silicon FETs grows increasingly challenging, alternative paths for improving digital system energy efficiency are being pursued. These paths include replacing the transistor channel with emerging nanomaterials (such as carbon nanotubes), as well as utilizing negative capacitance effects in ferroelectric materials in the FET gate stack, e.g., to improve sub-threshold slope beyond the 60 mV/decade limit. However, which path provides the largest energy efficiency benefits—and whether these multiple paths can be combined to achieve additional energy efficiency benefits—is still unclear. Here, we experimentally demonstrate the first negative capacitance carbon nanotube FETs (CNFETs), combining the benefits of both carbon nanotube channels and negative capacitance effects. We demonstrate negative capacitance CNFETs, achieving sub-60 mV/decade sub-threshold slope with an average sub-threshold slope of 55 mV/decade at room temperature. The average ON-current (I_{ON}) of these negative capacitance CNFETs improves by 2.1× versus baseline CNFETs, (i.e., without negative capacitance) for the same OFF-current (I_{OFF}). This work demonstrates a promising path forward for future generations of energy-efficient electronic systems.**

***Index Terms*— Negative capacitance, carbon nanotube, field-effect transistors, very-large-scale integration.**

I. Introduction

WHILE scaling FETs has improved energy efficiency of digital very-large-scale integrated (*VLSI*) circuits for decades (e.g., Dennard Scaling [1]), continued scaling is resulting in diminishing returns [2]. For instance, circuit supply voltage (V_{DD}) no longer scales according to Dennard Scaling, in part due to the sub-threshold slope (*SS*) limit of 60 mV/decade (at temperature = 300 °K) for conventional FETs (which in itself is difficult to achieve due to short-channel effects) [3], [4].

To overcome these challenges, multiple orthogonal paths are being pursued. One promising option is to replace today's silicon-based FET channels with ultra-thin body nanomaterials; for instance, carbon nanotubes (*CNTs*, Fig. 1b) can be used to realize carbon nanotube FETs (*CNFETs*, Fig. 1a), which offer superior electrostatic control vs. silicon-based FETs, simultaneously with superior carrier transport [5]. Another promising option is to introduce new materials into the FET gate stack; e.g., ferroelectric (*FE*) materials that exhibit negative capacitance (*NC*) can result in amplification of the electric field at the interface between the semiconductor channel and the gate oxide [6]. This allows the circuit supply voltage (V_{DD}) to decrease, thus lowering energy consumption while maintaining high effective gate-to-source voltage ($V_{GS,eff}$) for high drive current and high I_{ON}/I_{OFF} ratio (e.g., to improve energy efficiency) [7]. Importantly, NC can be combined with CNTs to realize NC-CNFETs, the focus of this manuscript.

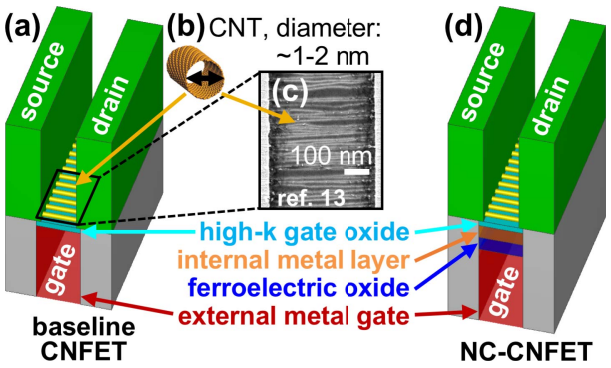

Fig. 1. (a) Schematic of baseline CNFET. (b) CNT. (c) Scanning electron microscope (SEM) of CNFET channel region (top view). (d) Schematic of NC-CNFET.

The schematic of an example NC-CNFET is shown in Fig. 1d (Fig. 1a: baseline CNFET: without negative capacitance). The gate stack (from bottom to top) consists of an external metal gate, a ferroelectric oxide, an internal metal layer, and a high-*k* gate oxide. Multiple parallel CNTs comprise the FET channel, whose conductance is modulated by the voltage of the internal metal layer; this layer serves to average the non-uniform charge in the NC-CNFET channel from source-to-drain under non-zero bias conditions, and presents an average charge to stabilize the ferroelectric capacitance in the negative capacitance state [8], [9]. The source, drain, and gate regions are defined using traditional photolithography.

Here, we experimentally demonstrate the first NC-CNFETs. For 100 single-CNT CNFETs (*i.e.*, CNFETs with a single CNT in the channel region), we show that our NC-CNFETs improve *SS* from an average of 70 mV/decade (for the baseline CNFETs) to an average of 55 mV/decade (for the NC-CNFETs), contributing to an average I_{ON} per CNT

Manuscript received November 13, 2017; revised December 5, 2017; accepted December 5, 2017. Date of publication December 11, 2017; date of current version January 25, 2018. This work was supported in part by Analog Devices, Inc., in part by DARPA under Grant W909MY-16-0001, and in part by the National Science Foundation under Grant CNS-1657303. The review of this letter was arranged by Editor Z. Chen. *(Corresponding author: Max M. Shulaker.)*

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Digital Object Identifier 10.1109/LED.2017.2781901

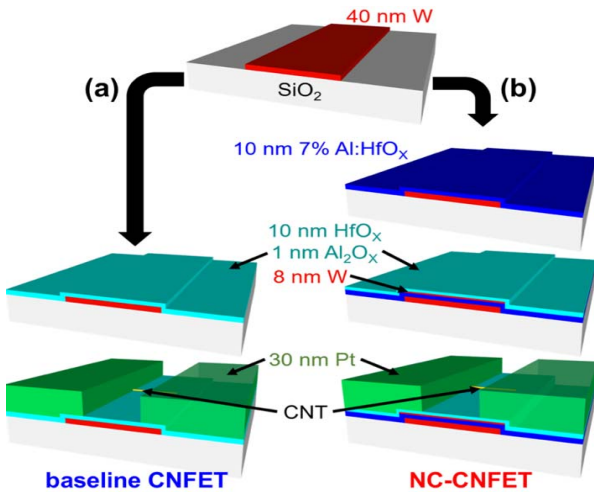

Fig. 2. Fabrication flow for (a) baseline CNFET & (b) NC-CNFET. The NC-CNFET gate stack consists of 40 nm tungsten (for the external metal gate), followed by 10 nm of ~7% aluminum-doped hafnium oxide (7% Al:HfO_X, deposited through atomic layer deposition). The Al:HfO_X exhibits ferroelectricity [8]. Next, 8 nm tungsten is deposited for the internal metal layer, followed by 10 nm of high-*k* HfO_X and 1 nm of aluminum oxide (Al_2O_X). The HfO_X deposited over the ferroelectric oxide ensures stable operation (e.g., positive gate capacitance), by introducing a positive capacitance dielectric oxide in series with the ferroelectric dielectric layer and the semiconductor [9], [10]. The 1 nm Al_2O_X provides an ideal surface for the subsequent transfer of CNTs over the channel region (after fabrication of the gate stack) [11]–[13]. Finally, platinum electrodes are deposited for source/drain.

increase of 2.1× versus baseline CNFETs for the same average I_{OFF}.

II. Fabrication Process

Fig. 2 illustrates the fabrication flow for baseline CNFETs (Fig. 2a) and NC-CNFETs (Fig. 2b). We use a back-gate FET geometry (*i.e.,* where the semiconducting channel of the FET is deposited over a pre-fabricated gate-stack), as it decouples the high temperature processing (>700 °C anneal) required for the ferroelectric material within the gate stack from the CNTs used as the channel [8]. The starting substrates for both baseline CNFETs and NC-CNFETs are silicon wafers with 800 nm of thermal SiO_2. For the back-gate, 40 nm of tungsten is defined through a lift-off process. For the NC-CNFET, a 10 nm ferroelectric dielectric is deposited, followed by a 8 nm tungsten metal layer. The ferroelectric dielectric is ~7% aluminum-doped hafnium oxide (7% Al:HfO_X), deposited through atomic layer deposition (ALD) at 200 °C, followed by a subsequent 800 °C anneal for 10 minutes. This ferroelectric dielectric has been studied extensively, and previous analysis on this dielectric can be found in ref. 8. Fig. 3 shows the polarization versus electric field (P-E) hysteresis loop of capacitors fabricated with 10 nm 7% Al:HfO_X dielectric and 10 nm HfO_X. Compared with the undoped HfO_X dielectric capacitor, the aluminum-doped HfO_X dielectric exhibits a P-E hysteresis loop, which confirms the ferroelectricity of the ALD grown thin film. The 8 nm tungsten deposited over the ferroelectric dielectric is an internal metal layer, and serves to average the non-uniform charge in the NC-CNFET channel from source-to-drain under non-zero bias conditions. This presents an average charge to stabilize the ferroelectric

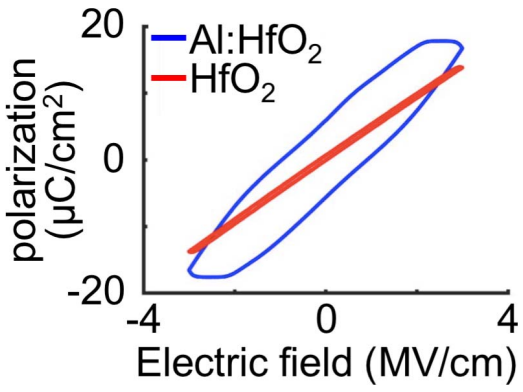

Fig. 3. Polarization versus electric field hysteresis capacitors made from 10 nm HfO_X dielectric, and 10 nm of 7% Al:HfO_X capacitors. The aluminum-doped HfO_X dielectric capacitor exhibits a P-E hysteresis loop, which confirms the ferroelectricity of the ALD grown thin film.

capacitance in the negative capacitance state [8], [9]. For both wafers (NC and otherwise), the remaining processing is identical. A 10 nm layer of HfO_X is deposited by ALD (over the ferroelectric gate stack for the NC-CNFET, and over the bare tungsten metal gate for the baseline CNFET). The HfO_X deposited over the ferroelectric oxide ensures stable operation (e.g., positive gate capacitance), by introducing a positive-capacitance dielectric oxide in series with the ferroelectric dielectric layer and the semiconductor [9], [10]. Following the 10 nm HfO_X, 1 nm Al_2O_X is deposited through ALD. The Al_2O_X provides an idea surface for the subsequent transfer of CNTs over the back-gates [11]–[13]. Chemical vapor deposition (CVD)-grown single-walled CNTs are transferred over the back-gates using the process described in ref. 13. Importantly, the transfer process is performed at low temperature (<120 °C), which avoids damaging the ferroelectric gate stack. The metal source and drain electrodes (0.5 nm titanium for adhesion followed by 40 nm platinum) are lithographically patterned and deposited through a lift-off process. Finally, mis-positioned CNTs outside of the channel region of the FETs are removed using oxygen plasma.

III. NC-CNFET Experimental Demonstration

We provide results from 100 CNFETs: 50 baseline CNFETs and 50 NC-CNFETs. The channel length of the CNFETs is 1 μm, and the width is chosen to achieve ~1 CNT per CNFET (to compare the performance of each single CNT channel). Each CNFET is first measured to determine if it has a semiconducting or a metallic CNT in the channel bridging the source and drain metal contacts (we define metallic CNTs as CNT that result in CNFETs with $I_{ON}/I_{OFF} < 100$; for energy-efficient circuits, metallic CNTs would be removed using techniques described in ref. 16). After measuring all of the CNFETs, we image each CNFET (using scanning electron microscopy (*SEM*)) to confirm that only a single semiconducting CNT is within the channel of the CNFET. SEM and cross-section transmission electron microscopy (*TEM*) images of a typical fabricated NC-CNFET are shown in Fig. 4 (in the TEM, individual CNTs are not visible due to the CNTs being perpendicular to the cross-section).

Fig. 5a shows $I_D - V_{GS}$ curves from 50 single-CNT baseline CNFETs and 50 single-CNT NC-CNFETs. The distributions

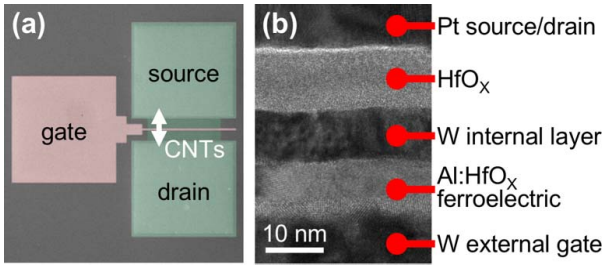

Fig. 4. NC-CNFET SEM (a) and cross-section TEM (b).

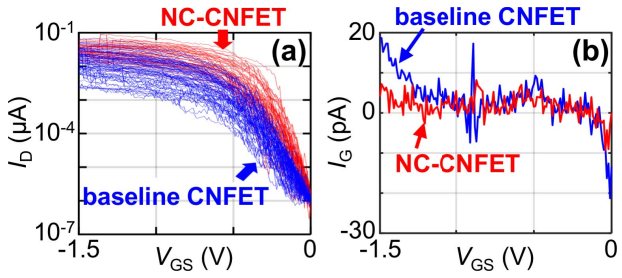

Fig. 5. Experimental measurements from 50 single-CNT baseline CNFETs and 50 single-CNT NC-CNFETs ($V_{DS} = 50$ mV). (a) I_D vs. V_{GS}. (b) Gate leakage (I_G) for one typical baseline CNFET and one typical NC-CNFET. Gate leakage is negligible, <30 pA.

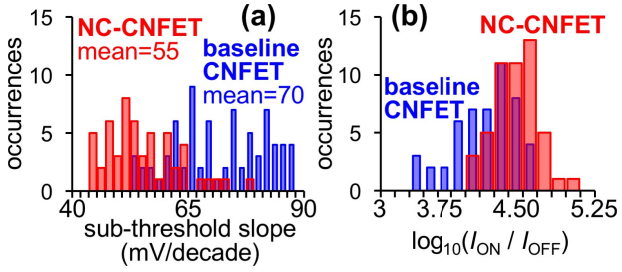

Fig. 6. Distributions of performance metrics for baseline CNFETs and NC-CNFETs (extracted from $I_D - V_{GS}$ curves shown in Fig. 5a). (a) Distribution of *SS* (*SS* is calculated over a 60 mV V_{GS} range). Baseline CNFETs exhibit mean *SS* of 70 mV/decade, while NC-CNFETs achieve mean *SS* of <60 mV/decade, with 55 mV/decade. (b) Distribution of I_{ON}/I_{OFF} (I_{ON} measured at $V_{GS} = -1.5$ V, I_{OFF} measured at $V_{GS} = 0V$. Average I_{ON}/I_{OFF} improves by 2.1× for NC-CNFETs compared to baseline CNFETs, for the same I_{OFF}.

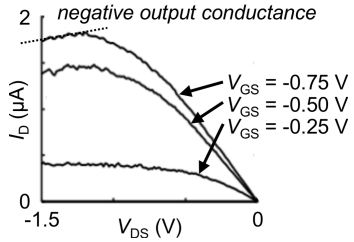

Fig. 7. $I_D - V_{DS}$ output characteristic of a typical NC-CNFET. Note the negative output conductance at high bias, e.g., for $V_{DS} = -1.5\ V$ with $V_{GS} = -0.75\ V$.

of *SS* and I_{ON}/I_{OFF} are shown in Fig. 6a and Fig. 6b respectively. The average *SS* improves from 70 mV/decade for baseline CNFET to 55 mV/decade for NC-CNFET. Due in part to the improved *SS*, the average I_{ON}/I_{OFF} improves by 2.1× for the same I_{OFF}. These results experimentally verify the effectiveness of the ferroelectric oxide to amplify the voltage of the external metal gate onto the internal metal layer and achieve sub-60 mV/decade *SS* operation. Importantly, gate leakage (I_G, which must be limited for stable negative capacitance operation [9]) is negligible ($|I_G| < 30$ pA) for both the baseline CNFETs and NC-CNFETs, is shown in Fig. 5b.

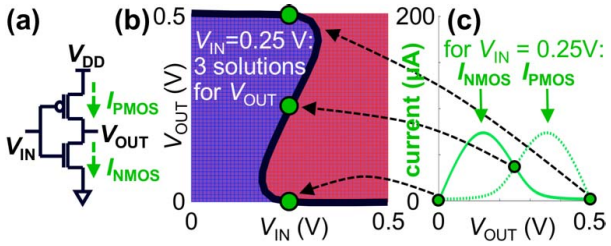

Fig. 8. Illustration of multiple solutions for DC convergence of logic gates built using NC-FETs, using a new SPICE-compatible compact model that combines the virtual source CNFET compact model [14] (for the FET current-voltage characteristics) with the NC gate stack from the MIT Virtual Source Negative Capacitance (MVSNC) model [15] (simulation result shown for an inverter built using NC-CNFETs with 5 nm FE oxide thickness). (a) Inverter schematic, indicating input voltage (V_{IN}), output voltage (V_{OUT}), PMOS current (I_{PMOS}) and NMOS current (I_{NMOS}). (b) Inverter voltage transfer curve (indicated by the thick black line), illustrating that multiple values of V_{OUT} can lead to DC convergence for a single value of V_{IN} (DC convergence: $I_{PMOS} = I_{NMOS}$). The multiple for solutions for DC convergence can result in hysteresis in logic gates (i.e., V_{OUT} can depend on previous values of V_{IN}), e.g., as discussed in ref. 21 and ref. 22. The shaded blue region indicates values of (V_{IN}, V_{OUT}) for which $I_{PMOS} > I_{NMOS}$ (and vice versa for the shaded red region). The green markers in (b) represent the three possible values of V_{OUT} for fixed $V_{IN} = 0.25$ V such that $I_{PMOS} = I_{NMOS}$; these correspond to the green markers in (c) , showing the values of V_{OUT} for which I_{PMOS} (dotted line) and I_{NMOS} (solid line) are equal.

Fig. 7 shows a typical $I_D - V_{DS}$ characteristic for an NC-CNFET. Importantly, while the NC-CNFET exhibits the expected saturation current as the magnitude of V_{DS} increases, it also exhibits negative output conductance (as shown in Fig. 7). This negative output conductance at high V_{DS} magnitude (which has been observed in NC-FET experimental demonstrations and is consistent with the expected behavior in the compact model as shown in Fig. 8c [15]) introduces a fundamental trade-off for NC-FETs: due to the non-monotonic relationship between I_D and V_{DS} in NC-FETs [15], there can be hysteresis in logic gates made from NC-FETs (illustrated in Fig. 8) [22], [23]. This is typically undesirable for digital logic circuits as it can lead to various circuit problems (e.g., incorrect logic functionality). Thus, the positive and negative capacitance portions of the gate stack must be carefully co-optimized to maximize energy efficiency benefits while minimizing the hysteric effect on logic gates.

IV. Conclusion

We have experimentally demonstrated the first NC-CNFETs, which achieve an average *SS* of 55 mV/decade (compared to 70 mV/decade for baseline CNFETs), and improve average I_{ON} by 2.1× versus baseline CNFETs (for the same I_{OFF}). This work experimentally demonstrates a path for combining the benefits of both CNT channels with negative capacitance effects, for future generations of energy-efficient electronic systems.

Acknowledgment

The authors thank Samuel Fuller of Analog Devices, Inc., for advice and collaborations.

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