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Role of Interfacial Oxide in High-Efficiency Graphene–Silicon Schottky Barrier Solar Cells

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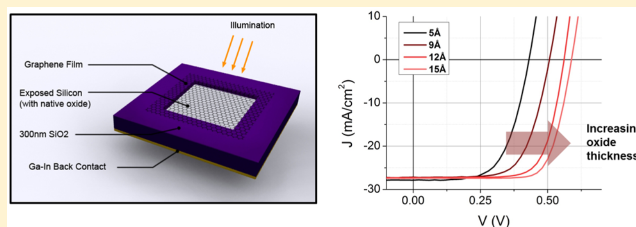
Supporting Information

ABSTRACT: The advent of chemical vapor deposition (CVD) grown graphene has allowed researchers to investigate large area graphene/n-silicon Schottky barrier solar cells. Using chemically doped graphene, efficiencies of nearly 10% can be achieved for devices without antireflective coatings. However, many devices reported in past literature often exhibit a distinctive s-shaped kink in the measured *I*/*V* curves under illumination resulting in poor fill factor. This behavior is especially prevalent for devices with pristine (not chemically doped) graphene but can be seen in some cases for doped graphene as well. In this work, we show that the native oxide on the silicon presents a transport barrier for photogenerated holes and causes recombination current, which is responsible for causing the kink. We experimentally verify our hypothesis and propose a simple semiconductor physics model that qualitatively captures the effect. Furthermore, we offer an additional optimization to graphene/n-silicon devices: by choosing the optimal oxide thickness, we can increase the efficiency of our devices to 12.4% after chemical doping and to a new record of 15.6% after applying an antireflective coating.



KEYWORDS: *graphene, solar cell, silicon, native oxide*

Because of its high electrical conductivity and optical transmittance, CVD graphene is a promising material for optoelectronic applications.[1−3] Transferring graphene onto silicon produces a Schottky junction, which can operate as a solar cell under illumination.[4,5] One reason silicon p−n solar cells remain dominant over their Schottky counterparts is that cheap screen-printed metal contacts can be used with the former, whereas the latter requires an evaporated metal grid.[6] Transferring CVD graphene is cheap and does not require high temperatures, making graphene a promising alternative for the top electrode of Schottky Barrier Solar Cells (SBSC's). Miao et al. demonstrates that polymer doping with trifluoromethanesulfonic acid (TFSA) can be used to improve the power conversion efficiency (PCE) of graphene−silicon devices to 8.6%.[7] Li et al. and An et al. independently showed that similar efficiencies can be achieved using other dopants.[8,9] More recently, it was shown that the addition of a TiO_2 antireflection coating further improves efficiency to 14.5%,[10] which still lags behind the best laboratory metal−insulation−semiconductor inversion layer (MIS-IL) solar cells (∼20%) but is not too far off from most commercial silicon solar cells (∼15%).[11] In several works involving graphene−silicon or CNT−silicon heterojunctions, there is a distinctive s-shaped kink (Figure 1c) in the *I*/*V* curve near the open-circuit voltage.[5,9,10,12−17] This kink is quite minor in some cases and very pronounced in others. As a result, many devices reported suffer from poor fill factor. In several cases, chemical doping or electrostatic gating mitigates or entirely suppresses this behavior.[10,12,13,17] Several past works offer explanations for this behavior. Wadhwa et al. hypothesizes that for electrolyte-gated CNT−silicon devices, this behavior arises from interface dipoles between the CNT's and silicon, whereas An et al. attribute the effect to the limited number of available states in graphene.[9,13] Jia et al. hypothesizes that the native oxide on silicon is responsible for this behavior in CNT−silicon devices and showed that the carrier transport mechanism changes from tunneling to thermionic emission as the oxide thickness increases.[18] Nevertheless, it is unclear which of the aforementioned mechanisms plays the dominant role in producing the kink in the *I*/*V* curves.

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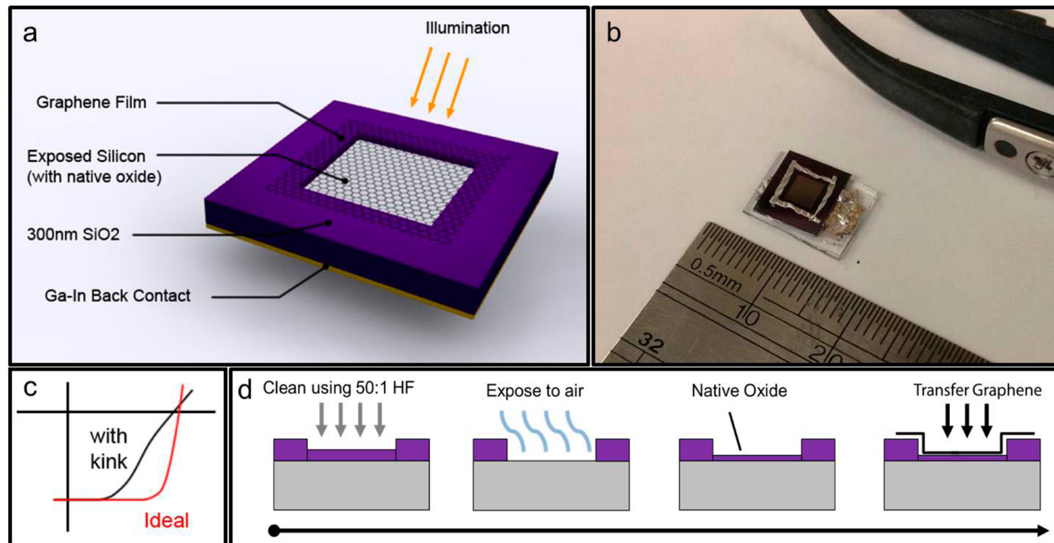

Figure 1. (a) Illustration of the device structure. (b) Photograph of device with 0.11 cm^2 area. Ruler scaled in cm. (c) Illustration of I/V curve with kink commonly found in past literature. (d) Schematic of device fabrication process.

In this work, we study this effect in detail for graphene/n-silicon devices. We observe, in agreement with Jia et al., that the kink becomes much more pronounced as the thickness of the native oxide between the silicon and graphene increases. Also, in agreement with previous results, we observe that the kink is more severe for higher illumination levels.[14,19] Furthermore, chemically doping the graphene suppresses the kink unless the oxide is too thick (>15 Å). We propose a model based on simple semiconductor physics that qualitatively explains the shape of the I/V curve and the effect of doping. Our model suggests that the combination of native oxide and the relatively low work function of graphene results in significant recombination current that suppresses photocurrent, resulting in the s-shaped kink. However, this understanding of the effect of the native oxide also suggests that we can improve the open circuit voltage of our devices by tuning the thickness of the oxide. Accordingly, we show that we can improve our device efficiency from 10.0% to 12.4% by applying this optimization. By the addition of an antireflective coating on top of the graphene layer, we can reliably achieve a PCE of 15.6%, which is the highest reported efficiency for graphene−silicon solar cells thus far.[10]

The device structure is shown in Figure 1a. A 0.11 cm^2 (3.33 × 3.33 mm) window was defined on 300 nm silicon oxide via photolithography and etched using buffered HF, exposing the lightly doped (2−4 Ωcm) n-type silicon. The devices are fabricated in large batches and stored in air for long periods of time. Before use, the devices were cleaned using a mixture of sulfuric acid and hydrogen peroxide (i.e., "piranha" etch) and the native oxide was removed by dipping the samples in diluted 50:1 HF for 30 s. The devices are then left in air for varying amounts of time to allow the native oxide to regrow. The oxide thicknesses were measured using an ellipsometer (Gaertner Scientific) accurate to ±3 Å.

It is well known that silicon grows a thin native oxide layer when exposed to ambient. From past literature, the thickness of this oxide is roughly 10 Å 1 h after HF treatment, increasing to 20 Å after 1 week and growing logarithmically with time thereafter.[20−22] From our experiences, the native oxide growth rate is a function of ambient humidity, but in general, we find that the thickness increases from ~5 Å immediately after HF treatment to ~15 Å after 2 weeks in air. To systematically study the effect of oxide thickness on the I/V characteristics, we leave our devices in air for varying lengths of time before transferring graphene (Figure 1d). As previously stated, we observe that a moderate oxide thickness (>9 Å) produces the distinctive kink. To explain these observations, we resort to basic semiconductor theory.

Light generates electron−hole pairs in the silicon; the electron−hole pairs in the graphene have much shorter lifetime (picoseconds) and are not considered here.[23] The built-in electric field at the Si−graphene interface separates the charges and pulls the holes toward the graphene. In the absence of an interfacial barrier, the holes are free to move into the graphene. However, if an oxide barrier is present, the holes will accumulate near the oxide−silicon interface. Because the number of electron−hole pairs generated is independent of barrier thickness, the flux of holes moving toward the junction is constant for a given illumination level, so the hole current density can be written as[20]

$$J_p = \frac{qD_p}{L_p}p' \quad (1)$$

where D_p and L_p are the characteristic diffusion coefficient and diffusion length for holes in silicon, respectively, and p' is the excess hole concentration in the bulk under illumination. These holes must either (1) tunnel through the barrier or (2) recombine with electrons through some mechanism. The hole tunnel current through the oxide can be expressed as[24]

$$J_t = \frac{4\pi m_{eff} q}{h^3 N_v}(kT)^2 p_s \exp(-\sqrt{\chi}\delta)\left(1 - \exp\left(-\frac{\Delta E_{fp}}{kT}\right)\right) \quad (2)$$

where m_{eff} is the effective mass of holes in the silicon, N_v is the effective density of states in the silicon valence band, p_s is the density of holes at the interface, χ is the average barrier height, δ is the oxide thickness, and ΔE_{fp} is the difference between the Fermi level in the graphene and the quasi-Fermi level for holes in the silicon under illumination. ΔE_{fp} and p_s are related by

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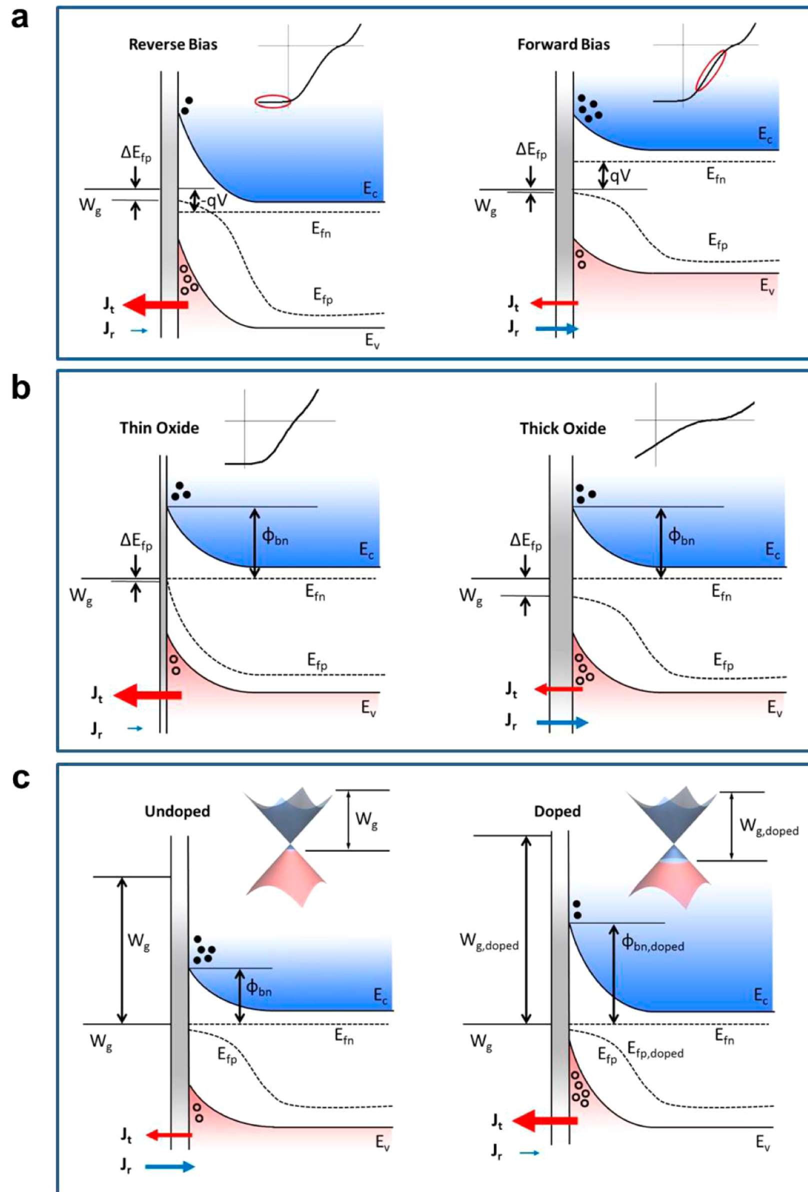

Figure 2. Energy band diagrams of a graphene/silicon heterojunction with an interfacial oxide under illumination. The size of the arrows indicates relative magnitudes of photocurrent (J_p) and recombination current (J_r). (a) Reverse bias versus forward bias. (b) Thin oxide versus thick oxide. (c) Pristine graphene versus doped graphene. The number of filled circles and hollow circles represents the relative abundance of electrons and holes in each case.

$$p_s = p_{s0} \cdot \exp\left(\frac{\Delta E_{fp}}{kT}\right) \tag{3}$$

where p_{s0} is the equilibrium hole concentration at the interface. Thus, ΔE_{fp} increases as p_s increases. Assume for now that all photogenerated holes must tunnel through the oxide, that is, $J_p = J_t$. We can equate eq 1 to eq 2 and observe how p_s changes as δ changes. For a very thin oxides ($\delta \sim 0$), the term exp $(-\sqrt{\chi_n}\delta)$ in eq 2 is roughly 1 so p_s (and therefore ΔE_{fp}) does not need to be large. As the oxide thickness increases, exp $(-\sqrt{\chi_n}\delta)$ decreases so p_s and ΔE_{fp} both need to increase to ensure $J_t = J_p$ (J_p is constant under constant illumination). Intuitively, for thicker oxides, holes will start to pile up near the interface while waiting to tunnel through.

However, if a large number of holes do accumulate near the interface, they will also tend to recombine with electrons. If the oxide is modestly thick (say, 15 Å), enough holes will accumulate near the interface and the surface carrier product $n_s p_s$ will then be much greater than the intrinsic carrier density n_i^2 and recombination will take place. Assuming a Shockley–Read–Hall model that captures recombination through trap states at the interface, the recombination rate for excess holes as a result of illumination can be approximated as[25]

$$R_T = \frac{n_s p_s - n_i^2}{\tau_{h0}(n_s + n_1) + \tau_{e0}(p_s + p_1)} \approx \frac{n_s p_s - n_i^2}{\tau(n_s + p_s)} \tag{4}$$

where $n_1 = N_C \exp((E_t - E_c)/kT)$ and $p_1 = N_V \exp((E_v - E_t)/kT)$ are related to the energy level of the trap states and E_t is the energy level of the trap states. We make the assumptions that the time constants for electrons and holes are roughly equal and that E_t is near the middle of the silicon band gap so $n_1 + p_1 \ll n + p$. From eq 4, we note that net recombination

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only takes place if the n_sp_s product is in excess of the intrinsic carrier product n_i^2. Furthermore, when there is an excess of carriers ($n_sp_s > n_i^2$), recombination is limited by the less abundant carrier. Thus, we have two competing processes: as surface hole concentration p_s increases, tunneling current increases but because n_sp_s increases, recombination current increases as well. Going back to our initial statement that photogenerated holes must go somewhere, we can say that equilibrium is established when the sum of recombination current and tunnel current is equal to photocurrent.

With this, we can qualitatively understand the I/V behavior caused by the interfacial layer. In reverse bias (Figure 2a), because of band-bending, the electron concentration at the interface is low. A large number of excess holes $p_s' = p_s - p_{s0}$ can accumulate near the interface because there are very few electrons with which they can recombine. ΔE_{fp} and p_s are large and photocurrent is equal to tunnel current. As we move into zero bias and small forward biases (Figure 2a), the electron concentration at the interface increases, and because recombination is limited by the less abundant carrier (in this case, electrons), recombination rate also increases. The excess hole concentration $p_{s'}$ will decrease because these holes will readily recombine with the many available electrons.

Where does the oxide thickness come into play? Assuming a very thin oxide, the term $\exp(-\sqrt{\chi}\delta)$ in eq 2 is close to 1 so very few excess carriers p_s' are necessary for J_t to equal J_p. Thus, $n_sp_s \approx n_i^2$ in eq 4 is small so recombination rate R_T is small unless n_s becomes very large (under significant forward bias). With a thicker oxide, however, more excess holes are necessary to push current through the oxide so p_s is larger. Therefore, n_s does not need to be as large for recombination to become significant, that is, recombination becomes significant at lower forward biases. These points are highlighted in Figure 2b.

Within the same framework, we can also understand why we can expect chemical doping to mitigate this effect. Doping increases W_g, which induces more band-bending at the interface (Figure 2c). The equilibrium interface hole concentration p_{s0} increases, whereas the corresponding electron concentration n_{s0} decreases proportionally. Because recombination is limited by the less-abundant carrier type (electrons), recombination current decreases for a given bias. Furthermore, eq 2 suggests that hole tunneling current is dependent on p_s. Thus, because the equilibrium hole concentration p_{s0} is higher, fewer *excess* holes are required for tunnel current to equal photocurrent so $p_s' = p_s - p_{s0}$ in eq 4 decreases. The combination of these two effects causes the forward bias at which recombination becomes significant to be pushed far to the right, into the forward regime of the diode, which effectively suppresses the kink. It is possible that because the screening from monolayer graphene is weak, as shown by Regan et al.,[16] $AuCl_3$ also induces p-type doping in the silicon. This would further increase depletion charge and lead to more band-bending at the interface, which would increase V_{oc} and thus enhance the performance.

This, of course, is a highly simplified model and we ignore many effects such as recombination in the silicon bulk and tunneling asymmetry between electrons and holes,[24] and the limited number of states in graphene.[9,14] Nonetheless, we will show that using this simple model, we can generate I/V curves that capture the essential features of the experimental data (detailed expressions in Supporting Information).

The I/V characteristics of the graphene/silicon devices under illumination were recorded after graphene transfer and thermal annealing; chemical doping was not applied for this set of devices. The sheet resistance of the undoped graphene was measured to be 400 Ω/sq. Figure 3a shows the I/V characteristics for these devices. As expected, as oxide thickness increases, the photocurrent suppression worsens and fill factor decreases. For most devices, the short circuit current density was 28 mA/cm^2; however, for the set of devices with the thickest oxide (22 Å), the photocurrent is suppressed even at short-circuit conditions and only settles to 28 mA/cm^2 given sufficient reverse bias. Figure 3b shows the set of I/V curves generated by our model and Figure 3c shows the recombination current (photocurrent minus tunnel current) of devices with moderately thick oxide along with the corresponding calculated curves. The recombination current fit is accurate for the range of biases relevant to the s-kink (approximately 0–0.55 V). Nevertheless, it can be also seen from Figure 3b that although the model works well for moderately thick oxides and predicts a correct trend as oxide thickness increases, it is not quantitatively accurate for even thicker oxides. In particular, the current increases much more gradually for the device with 22 Å oxide in the measured I/V curve than in the modeled curves.

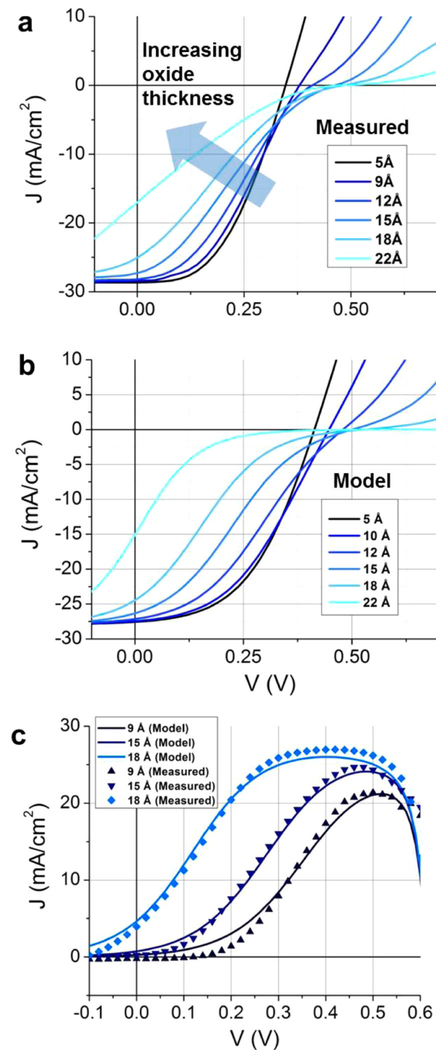

Figure 3. (a) I/V characteristics of graphene/n-silicon devices with varying oxide thicknesses before doping. (b) I/V curves of graphene/n-silicon devices generated from our model. (c) Comparison of recombination current for our model and measured data.

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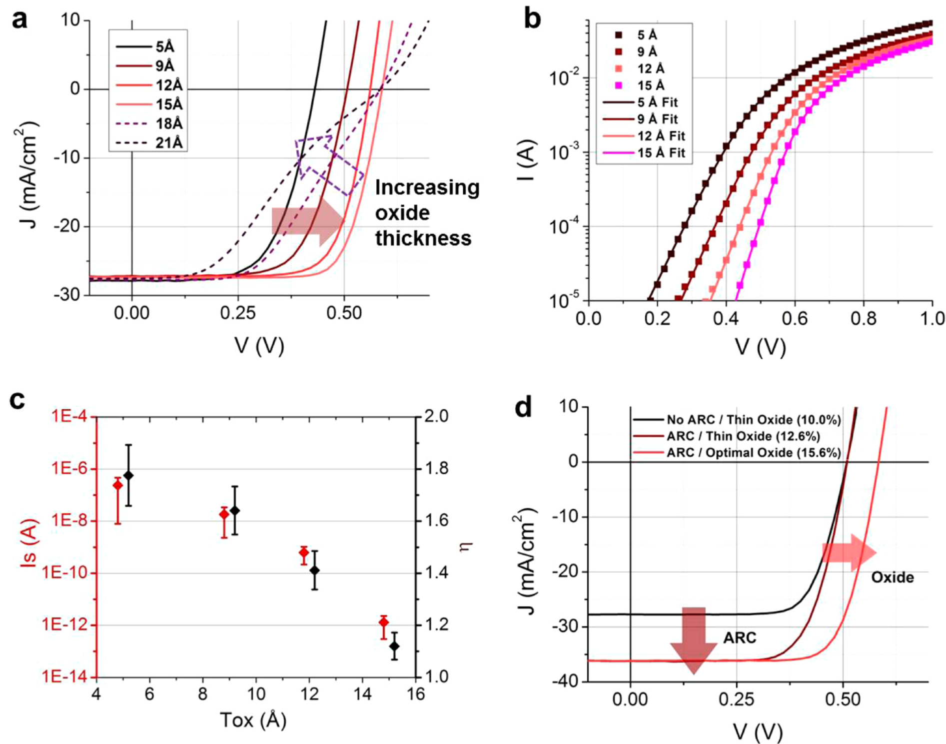

Figure 4. (a) I/V characteristics of graphene/n-silicon devices with varying oxide thicknesses after doping. (b) Measured and fitted I/V curves on a semilog scale. (c) Reverse saturation current I_S and ideality factor η as a function of oxide thickness. (d) Comparison of device with and without native oxide and antireflective coating (ARC).

From this discussion, it may be tempting to conclude that one should remove the native oxide completely. However, it has been reported that leaving the silicon exposed to air for some time before transferring graphene, thus allowing a moderately thick oxide to grow, yields optimal performance.[7] Researchers working on MIS solar cells in the 1970s also observed similar trends and eventually concluded that the native oxide layer improves presents a tunneling barrier for electrons, which reduces reverse saturation current and makes the diode less ideal in the forward regime.[20,26,27] Therefore, V_{oc} increases with oxide thickness, but making the oxide too thick results in photocurrent suppression; balancing these two phenomena was the key to achieving optical performance. For MIS devices, the optimal oxide thickness appears to be in the range of 15−25 Å.[28−30] The dark forward current can be expressed as

$$J_{tn} = \frac{4\pi m_{effn} q}{h^3}(kT)^2 \exp(-\sqrt{\chi_n}\delta)\exp\left(-\frac{q\phi_{bn}}{kT}\right)\exp\left(\frac{qV}{nkT}\right) \quad (5)$$

Equation 5 suggests that the Schottky diode forward current is simply reduced by the tunneling probability factor exp $(-\sqrt{\chi_n}\delta)$ as a result of the oxide. If we approximate the open-circuit voltage by equating forward current in eq 5 to photocurrent in eq 1 (which is constant under same illumination), we can immediately see that a thicker oxide will improve V_{oc}. Thus, it is clear that tuning the thickness of the native oxide layer is essential for maximizing device performance; we want the oxide layer to be as thick as possible in order to maximize V_{oc} while still thin enough that we can eliminate photocurrent suppression with chemical doping. We do a systematic study using devices with doped graphene to determine whether exposing to air for 2 h before transfer indeed results in this optimal oxide thickness.

The results are shown in Figure 4a. The sheet resistance of the graphene decreases to 120 Ω/sq after doping; the series resistance was extracted to be 9 ± 1.5 Ω for all devices with doped graphene (Supporting Information). A detailed discussion of the effect of series resistance and scaling can be found in the Supporting Information. Evidently, chemical doping suppresses the kink for all devices with oxide thickness up to 15 Å. From these curves, it is very obvious that V_{oc} increases for increasing oxide thickness. For devices left in air for 2 h before transfer, the average V_{oc} was 0.51 V and the average PCE was 10.0%, which is consistent with values reported for similar doped graphene/n-silicon devices reported in literature.[7,8,10] However, V_{oc} and PCE both increase further if the device is left in air longer before transfer. For the set of devices with 15 Å oxide, V_{oc} increases to 0.59 V and the average PCE increases to 12.4%, which represents a large improvement over past efforts mostly owing to the substantial increase in V_{oc}. For devices with oxide thicker than 15 Å, however, $AuCl_3$ doping is no longer sufficient to suppress the kink. Thus, we conclude that for our process, the optimal oxide thickness is roughly 15 Å, which agrees will with past results from MIS solar cells. The results are compiled in Table 1. As reported in past literature, $AuCl_3$-doped graphene degrades in air over time and as a result, the I/V characteristics of our devices revert to the undoped forms (with the s-kink) after 1 week.[10,31] Furthermore, we have found that graphene is not a perfect oxidation barrier and the native oxide continues to grow (albeit at a reduced rate) even after the silicon is covered with graphene. In the future, passivation to prevent both oxidation and doping reversion will be required to improve stability.

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Table 1. Summary of Performance Parameters of Devices under AM1.5 Illumination[a]

oxide thickness (Å)	J_{sc} (mA/cm^2)	V_{oc} (V)	fill factor	efficiency (%)
5	27.9	0.45	0.63	7.9
9	27.8	0.52	0.69	10.0
12	28.2	0.56	0.71	11.2
15	28.1	0.59	0.74	12.4
18	27.8	0.57	0.48	7.6
22	27.6	0.59	0.35	5.7
9w/ARC	36.8	0.52	0.66	12.6
15w/ARC	**36.7**	**0.595**	**0.72**	**15.6**

[a]Average values reported.

In order to extract parameters such as series resistance and reverse saturation current, we fit our measured I/V curves to a model of a diode with series resistance

$$I = I_s\left(\exp\left(\frac{q(V - IR_s)}{\eta kT}\right) - 1\right) \quad (6)$$

The reverse saturation current I_s, the ideality factor η, and the series resistance R_s are used as fitting parameters. The results of the fit are shown in Figure 4b and the fitted values for reverse saturation current and ideality factor are plotted in Figure 4c. The fitted series resistance values all fell in the range of 10−12 Ω (∼8−10 Ω/cm^2), which agrees well with the extracted values. Our fit shows that I_s decreases as oxide thickness increases, as predicted by eq 5. However, we find that η also decreases as oxide thickness increases, that is, the diode becomes more ideal, which is opposite to the behavior of gold/n-silicon Schottky diodes.[20,26,27] This observation is not well understood to us at this time. It has been shown that for metal−silicon Schottky diodes, trap states at the interface are responsible for lowering the ideality factor.[20] Sinha et al. recently demonstrated that the ideality factor of graphene−silicon Schottky junctions can be improved from 1.5 to 1.08 by removing surface impurities on copper before graphene growth.[32] From these results, we hypothesize that thicker oxides better passivate the silicon surface, thereby reducing the number of interface trap states and making the device more ideal. Nonetheless, the decrease in I_s is sufficient to improve the open-circuit voltage of our devices as the oxide thickness increases in spite of the decrease in ideality factor.

We also apply a TiO_2 antireflective coating (ARC) to our devices following the procedure described by Shi et al.[10] For devices with optimal oxide thickness, J_{sc} increases to 37 mA/cm^2 and V_{oc} increases marginally to 0.595 V, whereas fill factor decreases slightly to 0.72 (Figure 4d). The overall efficiency is 15.6%, which is the best value reported in literature thus far. Devices with an ARC but a thin oxide (9 Å after leaving in air for 2 h) have V_{oc} of 0.52 V and efficiency of 12.6%. Compared to the devices reported by Shi et al.,[10] our devices have slightly lower V_{oc} but higher J_{sc} due to the lower doping levels of our silicon.

In summary, as we get closer to theoretical limits for solar cells, we quickly encounter diminishing returns with effort and it becomes necessary to better understand the intricacies in our devices in order to optimize performance. Here, we investigated the role of the native silicon oxide layer in graphene−silicon Schottky barrier solar cells. We propose that the current through these devices under illumination is determined by a balance between tunneling and recombination. As oxide thickness increases, recombination dominates over tunneling and the s-shaped kink in the I/V characteristics of these devices becomes more apparent, resulting in reduced fill factor. Chemical doping raises the work function of graphene and reduces recombination, thereby suppressing the kink for oxide thickness less than 15 Å. Additionally, the reverse saturation current decreases by several orders of magnitude as oxide thickness increases from 5 to15 Å, resulting in higher V_{oc} for devices with thicker oxides. Our understanding of the role of the interfacial oxide is an important step in reliably achieving the current best PCE of 15.6% in graphene−silicon devices. This optimization also suggests possible routes for future improvement. For example, heavier doping might further increase the optimal oxide thickness, leading to even greater V_{oc}, as well as better fill factor due to enhanced conductivity in graphene; a better antireflective coating (the refractive index of our TiO_2 was measured to be 1.7 instead of the optimal 2.0) will provide greater J_{SC}. In the 1970s, Schottky solar cells were widely studied because they did not require a high-temperature diffusion and, therefore, could potentially be fabricated using lower quality polycrystalline silicon.[6] However, it was found that Schottky devices are highly sensitive to the metal−silicon interface and tend to drift over time. It is uncertain at this time whether graphene−silicon devices experience similar problems but this area of research may be worth revisiting from an industrial standpoint. Furthermore, this understanding of the graphene−semiconductor interface can be applied to other emerging 2D material heterostructures. For example, researchers have proposed Schottky solar cells based on graphene−MoS_2 heterojunctions.[33] We might consider what would happen if we insert a monolayer of insulated h-BN between the graphene and MoS_2; would such a structure experience similar enhancements in efficiency? Because silicon oxidizes in air, graphene−silicon heterojunctions is a convenient structure for studying the effect of insulating layer but in the future, we can develop the tools necessary to study this in the context of other novel materials.

Experimental Section. *Device Fabrication and Characterization.* Monolayer graphene was grown on copper foil (JX Metals & Mining) using LPCVD and transferred over the silicon window using the standard PMMA transfer method reported in literature.[2] The PMMA was removed by immersing in acetone for 20 min followed by thermal annealing at 350 °C for 2 h in a hydrogen/argon environment. Gallium−indium eutectic (99.99% Sigma-Aldrich) was used as the back silicon contact and a ring of indium wire was laid around the active area to contact the graphene. The graphene was p-doped by spin-casting $AuCl_3$ dissolved (10 mM) in nitromethane at 2500 rpm.

Sheet resistances were measured using Van der Pauw's method with an HP 4155A semiconductor parameter analyzer and a home-built four point probe station. Device current/voltage (I/V) curves were measured under AM1.5 illumination (100 mW/cm^2) with a Keithley 2602 SourceMeter.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

Effect of series resistance and device scaling, model details, and extracting series resistance. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Li, X.; Cai, W.; An, J.; Kim, S.; Nah, J.; Yang, D.; Piner, R.; Velamakanni, A.; Jung, I.; Tutuc, E.; Banerjee, S. K.; Colombo, L.; Ruoff, R. S. *Science* **2009**, *324*, 1312−4.

(2) Reina, A.; Jia, X. T.; Ho, J.; Nezich, D.; Son, H. B.; Bulovic, V.; Dresselhaus, M. S.; Kong, J. *Nano Lett.* **2009**, *9*, 30−35.

(3) Bae, S.; Kim, H.; Lee, Y.; Xu, X. F.; Park, J. S.; Zheng, Y.; Balakrishnan, J.; Lei, T.; Kim, H. R.; Song, Y. I.; Kim, Y. J.; Kim, K. S.; Ozyilmaz, B.; Ahn, J. H.; Hong, B. H.; Iijima, S. *Nat. Nanotechnol.* **2010**, *5*, 574−578.

(4) Chen, C. C.; Aykol, M.; Chang, C. C.; Levi, A. F. J.; Cronin, S. B. *Nano Lett.* **2011**, *11*, 1863−1867.

(5) Li, X. M.; Zhu, H. W.; Wang, K. L.; Cao, A. Y.; Wei, J. Q.; Li, C. Y.; Jia, Y.; Li, Z.; Li, X.; Wu, D. H. *Adv. Mater.* **2010**, *22*, 2743−2748.

(6) Townsend, W. G. *IEE J. Solid-State Electron Devices* **1978**, *2*, S31−S34.

(7) Miao, X. C.; Tongay, S.; Petterson, M. K.; Berke, K.; Rinzler, A. G.; Appleton, B. R.; Hebard, A. F. *Nano Lett.* **2012**, *12*, 2745−2750.

(8) Li, X. M.; Xie, D.; Park, H.; Zhu, M.; Zeng, T. H.; Wang, K. L.; Wei, J. Q.; Wu, D. H.; Kong, J.; Zhu, H. W. *Nanoscale* **2013**, *5*, 1945−1948.

(9) An, X.; Liu, F.; Kar, S. *Carbon* **2013**, *57*, 329−337.

(10) Shi, E.; Li, H.; Yang, L.; Zhang, L.; Li, Z.; Li, P.; Shang, Y.; Wu, S.; Li, X.; Wei, J.; Wang, K.; Zhu, H.; Wu, D.; Fang, Y.; Cao, A. *Nano Lett.* **2013**, *13*, 1776−1781.

(11) Hezel, R. *Sol. Energy Mater. Sol. Cells* **2002**, *74*, 25−33.

(12) Shi, Y. M.; Kim, K. K.; Reina, A.; Hofmann, M.; Li, L. J.; Kong, J. *ACS Nano* **2010**, *4*, 2689−2694.

(13) Wadhwa, P.; Liu, B.; McCarthy, M. A.; Wu, Z. C.; Rinzler, A. G. *Nano Lett.* **2010**, *10*, 5001−5005.

(14) An, X. H.; Liu, F. Z.; Jung, Y. J.; Kar, S. *Nano Lett.* **2013**, *13*, 909−916.

(15) Wadhwa, P.; Seol, G.; Petterson, M. K.; Guo, J.; Rinzler, A. G. *Nano Lett.* **2011**, *11*, 2419−2423.

(16) Regan, W.; Byrnes, S.; Gannett, W.; Ergen, O.; Vazquez-Mena, O.; Wang, F.; Zettl, A. *Nano Lett.* **2012**, *12*, 4300−4304.

(17) Li, X. M.; Xie, D.; Park, H.; Zeng, T. H.; Wang, K. L.; Wei, J. Q.; Zhong, M. L.; Wu, D. H.; Kong, J.; Zhu, H. W. *Adv. Energy Mater.* **2013**, *3*, 1029−1034.

(18) Jia, Y.; Cao, A.; Kang, F.; Li, P.; Gui, X.; Zhang, L.; Shi, E.; Wei, J.; Wang, K.; Zhu, H.; Wu, D. *Phys. Chem. Chem. Phys.* **2012**, *14*, 8391−8396.

(19) Anderson, R. L. *Appl. Phys. Lett.* **1975**, *27*, 691−693.

(20) Card, H. C.; Rhoderic, Eh. *J. Phys. D: Appl. Phys.* **1971**, *4*, 1589−1601.

(21) Morita, M.; Ohmi, T.; Hasegawa, E.; Kawakami, M.; Ohwada, M. *J. Appl. Phys.* **1990**, *68*, 1272−1281.

(22) Raider, S. I.; Flitsch, R.; Palmer, M. J. *J. Electrochem. Soc.* **1975**, *122*, 413−418.

(23) Limmer, T.; Feldmann, J.; Da Como, E. *Phys. Rev. Lett.* **2013**, *110*, 217406.

(24) Ng, K. K.; Card, H. C. *J. Appl. Phys.* **1980**, *51*, 2153−2157.

(25) Shockley, W.; Read, W. T. *Phys. Rev.* **1952**, *87*, 835−842.

(26) Lillington, D. R.; Townsend, W. G. *Appl. Phys. Lett.* **1976**, *28*, 97−98.

(27) Card, H. C. *Solid-State Electron.* **1977**, *20*, 971−976.

(28) Viktorovitch, P.; Pananakakis, G.; Kamarinos, G.; Basset, R. Determination of optimum parameters and characterization of MIS solar cells. *IEEE Int. Electron Devices Meet.* **1977**, 62.

(29) Ng, K. K.; Card, H. C. Photocurrent suppression and interface state recombination in MIS-Schottky barriers. *IEEE Int. Electron Devices Meet.* **1977**, 57−61.

(30) Viktorovitch, P.; Kamarinos, G. *J. Appl. Phys.* **1977**, *48*, 3060−3064.

(31) Kim, K. K.; Reina, A.; Shi, Y.; Park, H.; Li, L. J.; Lee, Y. H.; Kong, J. *Nanotechnology* **2010**, *21*, 285205.

(32) Sinha, D.; Lee, J. U. *Nano Lett.* **2014**, *14*, 4660−4664.

(33) Bernardi, M.; Palummo, M.; Grossman, J. C. *Nano Lett.* **2013**, *13*, 3664−3670.