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Subthreshold swing improvement in MoS_2 transistors by the negative-capacitance effect in a ferroelectric Al-doped-HfO_2/HfO_2 gate dielectric stack

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Obtaining a subthreshold swing (SS) below the thermionic limit of 60 mV dec^{-1} by exploiting the negative-capacitance (NC) effect in ferroelectric (FE) materials is a novel effective technique to allow the reduction of the supply voltage and power consumption in field effect transistors (FETs). At the same time, two-dimensional layered semiconductors, such as molybdenum disulfide (MoS_2), have been shown to be promising candidates to replace silicon MOSFETs in sub-5 nm-channel technology nodes. In this paper, we demonstrate NC MoS_2 FETs by incorporating a ferroelectric Al-doped HfO_2 (Al : HfO_2), a technologically compatible material, in the FET gate stack. Al : HfO_2 thin films were deposited on Si wafers by atomic layer deposition. Voltage amplification up to 1.25 times was observed in a FE bilayer stack of Al : HfO_2/HfO_2 with a Ni metallic intermediate layer. The minimum SS (SS_{min}) of the NC-MoS_2 FET built on the FE bilayer improved to 57 mV dec^{-1} at room temperature, compared with SS_{min} = 67 mV dec^{-1} for the MoS_2 FET with only HfO_2 as a gate dielectric.

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Introduction

For decades, computer chips have been solely made of silicon. However, doubling the number of chips on the same integrated circuit area, and thus following Moore's law, is becoming increasingly challenging as silicon technology reaches its physical limit. Two main paths are currently being pursued to continue the scaling of CMOS technology in the next few decades: 1. finding a new channel material that would allow electronics to move beyond silicon in miniaturization of the transistor channel length, and 2. determination of a new device mechanism to overcome the thermionic limit in metal oxide semiconductor field effect transistors (MOSFETs), thereby enabling reduction of the power consumption by further reducing the supply voltage.

Recently, layered two-dimensional (2D) semiconducting crystals of transition metal dichalcogenides (TMDs), such as molybdenum disulfide (MoS_2) and tungsten diselenide (WSe_2), have been proposed to enable aggressive miniaturization of FETs.[1–4] The atomically-thin body thickness of TMDs improves the gate modulation efficiency. This can be seen in their characteristic scaling length,[5] $\lambda = \sqrt{\frac{\varepsilon_{semi}}{\varepsilon_{ox}} t_{ox}.t_{semi}}$, where $\varepsilon_{semi}/t_{semi}$ and ε_{ox}/t_{ox} are the dielectric constant/thickness of the channel and oxide, respectively. λ determines important short channel effects such as drain-induced barrier lowering and the subthreshold swing (SS). In particular, MoS_2 has a low dielectric constant of ε = 4–7 (ref. 6 and 7) and an atomically thin body ($t_{semi} \approx 0.7$ nm × number of layers), which facilitate the decrease of λ, while its relatively high bandgap energy (1.85 eV for a monolayer) and high effective mass allow for a high on/off current ratio (I_{on}/I_{off}) *via* reduction of direct source–drain tunneling.[8] These features make MoS_2, and wide-bandgap 2D semiconductors in general, interesting candidates for low-power subthreshold electronics.

We have previously reported methods to reduce the channel length in MoS_2 FETs to 15 nm using graphene contacts[3] and 7.5 nm using directed self-assembly patterning.[9] Despite the advances made in TMD FET miniaturization, the power scaling in such devices suffers from the same issues than in Si MOSFET technology, where the supply voltage is limited by SS, which is the gate voltage change (ΔV_g) required to increase the source–drain current (I_{ds}) by one decade:

$$SS = \frac{dV_g}{d\psi_s} \times \frac{d\psi_s}{d(\log I_{ds})}, \quad \frac{dV_g}{d\psi_s} = \left(1 + \frac{C_s}{C_{ins}}\right)$$

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where C_s and C_{ins} are the semiconductor and dielectric insulator capacitance, k is the Boltzmann constant, T is the temperature, and q is the elementary charge.

Limited by thermionic emission, Boltzmann statistics limits the second term in the above formula to $\ln(10)kT/q$, which is about 60 mV dec^{-1} at room temperature. The first term, which is known as the body factor m, is always greater than one. Therefore, SS > 60 mV dec^{-1} at room temperature in a standard MOSFET, limiting the minimum supply voltage possible for a given drain current capability. To lower the SS and, in that way, the supply power, we need to overcome the limit of at least one of the terms in the above formula.

To overcome the limit of $\frac{d\psi_s}{d(\log I_{ds})}$ a transport mechanism different from thermionic emission is required. The most widely studied method is tunnel-FETs, where carriers are injected into the channel by band-to-band tunneling from the source to the drain so over-barrier emission, as in MOSFETs, is circumvented. This allows steeper change of the current and thus overcomes the limit of 60 mV dec^{-1}. However, the experimental results reported so far severely suffer from the interface trap assisted tunneling mechanism, which generates a large background current obscuring the steepness of turn on of the band-to-band tunneling.[10]

An alternative method to reduce the SS below 60 mV dec^{-1} in a MOSFET is to decrease the body factor to less than one.[11] This requires the capacitance to be mathematically negative (*i.e.*, $C_{ins} < 0$). The body factor is the inverse of the gate efficiency ($\beta = d\psi_s/dV_g$), which is the rate that the semiconductor surface potential ψ_s changes by changing V_g. Therefore, if $C_{ins} < 0$ then $\beta > 1$, a condition that is always impossible with conventional dielectric insulators.

A negative differential capacitance effect has been experimentally observed in ferroelectric materials during the phase transition when the system is in nonequilibrium.[12] In addition, sub-60 mV dec^{-1} switching characteristics have been observed in several negative-capacitance (NC) FETs using lead zirconate titanate,[13] bismuth ferrite[14] and polymer ferroelectric dielectrics such as P(VDF)-TRFE.[15,16] However, neither of these materials is technologically compatible with standard Si CMOS technology. In this regard, HfO_2 and ZrO_2[17] based ferroelectric materials are more favorable because they are fully compatible with the CMOS manufacturing process and their thin films can be obtained by standard deposition techniques, such as atomic layer deposition (ALD), and they can thus be easily integrated into transistor structures. The HfO_2-based gate dielectric has been extensively developed for CMOS applications with well-defined ALD processing technology, and it is used in current technology nodes. In addition, robust ferroelectricity has been reported in thin-films of HfO_2 systems with various dopants, such as rare-earth,[18] Si,[19] and Al[20] dopants. Here, we used Al-doped HfO_2 (Al : HfO_2) ferroelectric thin films to develop NC-MoS_2 FETs. We believe that incorporation of the NC mechanism in transistors with a 2D channel (*e.g.*, MoS_2 FETs) could be a solution to extend the boundaries of transistor dimension scaling as well as power scaling, and extend Moore's law to its ultimate limit to enable the continued increase of the functionality of semiconductor electronics.

Results and discussion

The atomic accuracy in the thickness of ALD films allows precise control of the molar ratio of the dopant to the host metal in bimetal oxide systems such as Al : HfO_2. In our work, ALD Al : HfO_2 deposition was carried out at a substrate temperature of 250 °C using trimethylaluminum (TMA) as the Al precursor, tetrakis(ethylmethylamino)hafnium (TEMAH) as the Hf precursor, and H_2O as the oxidant. A Si wafer with a native SiO_2 layer was used as the substrate. The Al composition of the films was varied from 0% to 16.7% by controlling the TMA/TMHA pulses. The ALD process consisted of TMA cycles in the middle of sequences of TEMAH cycles. After deposition, the samples were rapid thermal annealed (RTA) in forming gas at 850 °C for 5 min to crystallize the films and intermix Al with the HfO_2 body to form a homogenous Al : HfO_2 matrix.

XPS analysis was performed on the Al : HfO_2 films after varying the ratio of TMA cycles to TEMAH cycles (Fig. 1(a) and (b)). Fig. 1(c) shows a plot of the Al content of ~10 nm thin films extracted from the XPS analysis *versus* the TMA/TEMAH cycle ratio. The linear fit with near unity slope shows that the Al content can be precisely controlled in the range 0%–16.7%. Moreover, in-depth analysis showed negligible variation in the Al content after different etching times by Ar plasma, which indicates that the Al dopant atoms are uniformly dispersed in the HfO_2 lattice.

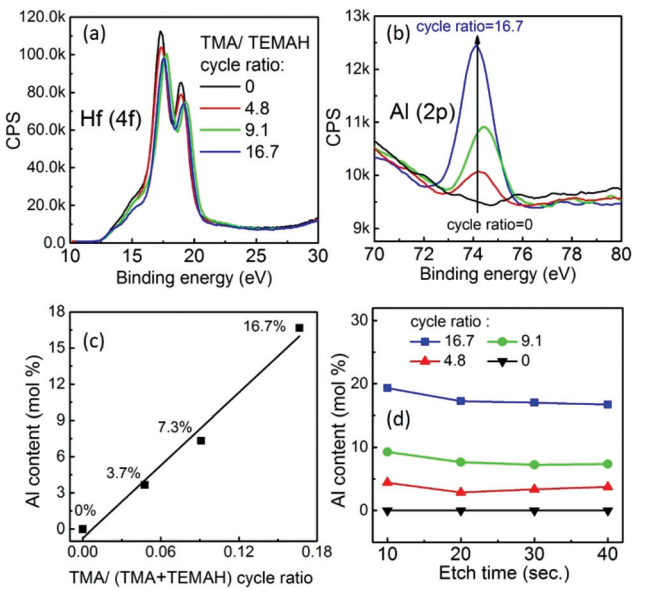

Fig. 1 (a) and (b) XPS analysis of Al-doped HfO_2 films with different Al contents deposited on Si wafers with TMA/TEMAH cycle ratios ranging from 0 to 16.7%. (c) Al content of the Al : HfO_2 films extracted from the XPS spectra shown in (a) and (b) as a function of the TMA/TEMAH cycle ratio. The inset shows as a schematic of the deposited stacked HfO_2 and Al_2O_3 and homogeneously Al-doped HfO_2 (Al : HfO_2) formed after RTA. (d) Al contents for different etch times.

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Fig. 2(a) compares the grazing incident X-ray diffraction (GIXRD) patterns of the undoped and 7.3% Al : HfO_2 samples. The XRD analysis suggests a phase transition from the monoclinic phase to the orthorhombic phase upon doping. This noncentrosymmetric transition phase is a prerequisite for ferroelectric characteristics. See ref. 17 for more detail on different phases of Al : HfO_2. Next, we analyzed the ferroelectric capacitor with a 10 nm 7.3% Al : HfO_2 film. For this measurement, a highly doped Si wafer was used as the back electrode and Ni pads were patterned on the thin film as the top electrode. An extra RTA step was performed at 450 °C after deposition of the Ni electrodes to eliminate charged interfacial trapped states.

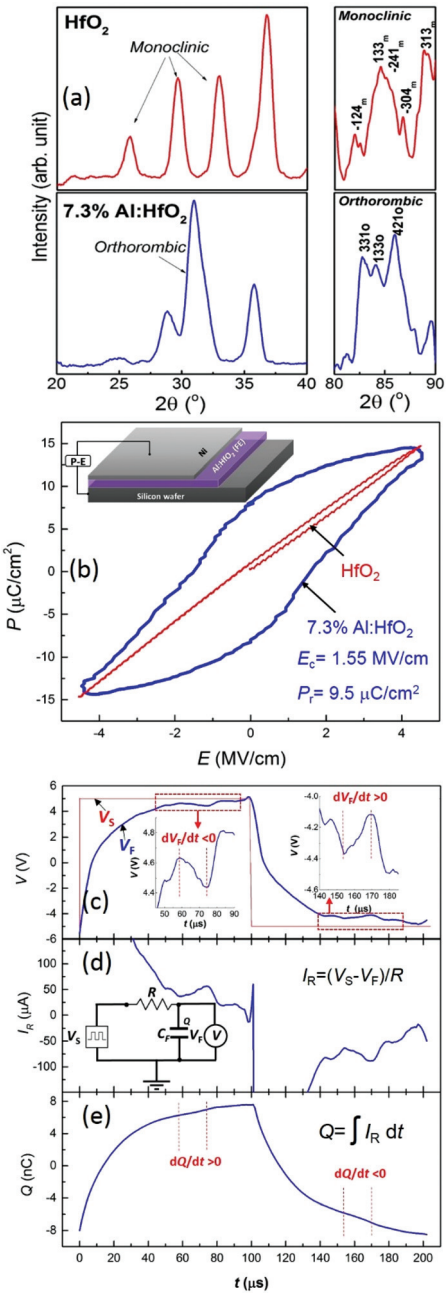

Fig. 2 (a) GIXRD patterns of undoped and 7.3% Al-doped HfO_2. (b) Polarization *versus* electric field hysteresis of undoped and 7.3% Al-doped HfO_2. (c–e) Transient voltage, current, and charge of 10 nm 7.3% Al-doped HfO_2 with a 200 μs period. The insert of (d) shows a schematic of the measurement setup.

Fig. 2(b) shows plots of the polarization *versus* electric field (*P–E*) hysteresis loop of 10 nm 0% and 7.3% Al : HfO_2 capacitors. Compared with the undoped sample, the 7.3% sample shows a *P–E* hysteresis loop, which confirms the ferroelectricity of the ALD grown thin film with a coercive field of 1.55 MV cm^{-1} and remnant polarization of 9.5 μC cm^{-2}. Fig. 2(c)–(e) show the transient voltage (V_F), current (I_R), and charge (Q) of the capacitor on application of a square voltage pulse (V_s). A schematic of the measurement setup is shown in the insert of Fig. 2(d). I_R is determined by $I_R = (V_s - V_F)/R$, where R is a 10 kΩ resistor and Q is calculated using $Q = \int I_R(t)dt$. The regions of interest are marked with dashed lines in Fig. 2(c) and (e), where V_F and Q show different trends and dV_F/dt and dQ/dt have opposite signs. This indicates the presence of a negative capacitance feature in these regions ($C = dQ/dV < 0$).

As previously discussed, the aim of incorporating a ferroelectric material in the gate stack of a MOSFET is to increase the gate efficiency above one by exploiting the NC effect of the ferroelectric material. Regardless of its absolute value, any NC can make the gate efficiency greater than one. However, it should be noted that the total gate capacitance C_g has to remain positive to avoid instability in the system, which requires that $|C_f| > C_s$ (where C_f is the ferroelectric NC), otherwise it will result in strong hysteresis during device operation.[21] This condition can fail because C_s is a nonlinear function of V_g and V_d, which can push the transistor to an instable condition during its transition from depletion (low C_s) to the inversion condition (high C_s). To guarantee positive C_g in the whole operation regime, a positive-capacitance dielectric oxide (C_{ox}) can be added in series with the ferroelectric dielectric layer and the semiconductor. In this bilayer configuration, $|C_f|$ has to be greater than the oxide dielectric capacitance ($|C_f| > C_{ox}$) to amplify the gate efficiency ($\beta > 1$) and greater than $C_{mos} = (C_s^{-1} + C_{ox}^{-1})^{-1}$ to meet the stability condition ($C_g > 0$), which is always the case as long as the first condition ($|C_f| > C_{ox}$) is met. However, despite this theoretical conditions for stabilization of NC, it should be noted that in a bilayer gate stack, the presence of any finite gate leakage does not allow NC full stabilization.[22] Nevertheless if the gate voltage is ramped up faster than the time required to discharge the capacitance (RC delay), the transistor can enter the NC regime.

Here, we used undoped HfO_2 as the positive-capacitance oxide component in the bilayer gate stack. To protect the surface potential in the device against the charge nonuniformity induced by microdomains in the ferroelectric film, the ferroelectric and the normal dielectric layers need to be separated by a metal layer to average out such non-uniformities.[23] To evaluate the potential amplification in the bilayer structure, we fabricated a test capacitor structure composed of Ni pads formed on the 10 nm 7.3% Al : HfO_2/Si substrate, a 10 nm HfO_2 layer deposited on the Ni pads by ALD, and Au top elec-

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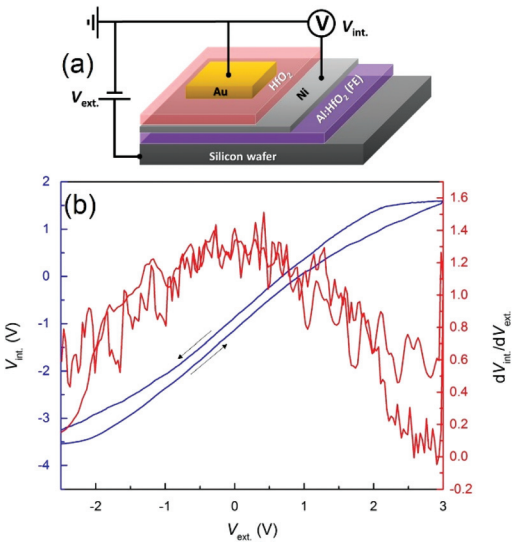

Fig. 3 (a) Schematic of the measurement setup used to characterize the potential amplification in the nominal 10 nm-Al : HfO_2/10 nm-HfO_2 bilayer system with a Ni intermediate electrode. V_{ext} was applied to the Si wafer and the induced potential on the intermediate Ni electrode V_{int} was read in voltage mode (voltmeter). (b) V_{int} and dV_{int}/dV_{ext} *versus* V_{ext}.

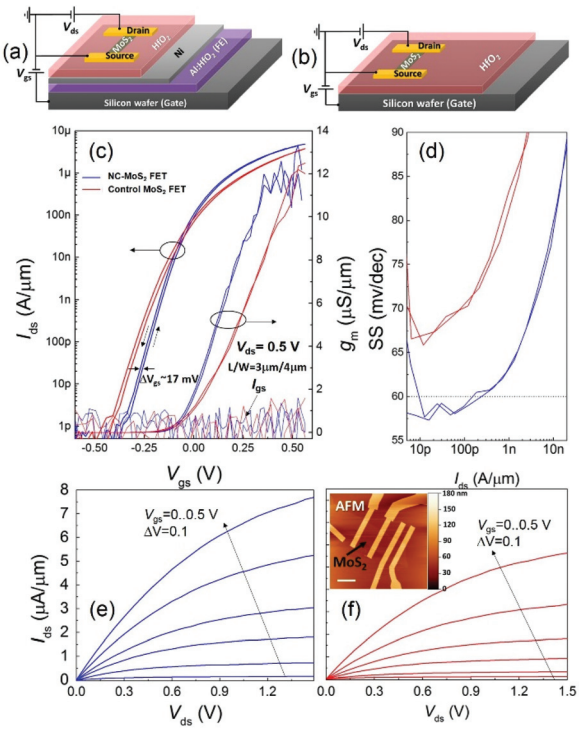

Fig. 4 (a) Schematic of the NC-MoS_2 FET with a HfO_2/Al : HfO_2 bilayer stack with Ni used as the intermediate metal. (b) Schematic of a reference regular MoS_2 FET with a HfO_2 gate dielectric. In both (a) and (b), a highly doped Si wafer is used as the back gate. (c) Transfer characteristics and transconductance of the NC-MoS_2 FET and reference MoS_2 FET at room temperature. (d) Comparison of the SS of the NC-MoS_2 FET with that of the reference MoS_2 FET. (e), (f) Output characteristics of NC-MoS_2 FET and control MoS_2 FET, respectively. The inset in (f) shows an AFM image of a MoS_2 FET. The scale bar is 4 μm.

trodes deposited on the HfO_2 layer (see Fig. 3(a)). In the device, contact holes were etched through HfO_2 to access the intermediate Ni layer.

Fig. 3(b) shows a plot of the potential of the intermediate Ni electrode V_{int} *versus* the potential applied to the doped-Si substrate, V_{ext}, when the top electrode is grounded. This shows how much V_{int} can be amplified by the NC effect. Using the capacitor divider method, the amplification factor is $dV_{int}/dV_{ext} = [1/(1 + C_{ox}/C_f)]$. The factor monotonically increases, exceeds one at $V_{ext} \sim -1.5$ V, and reaches an average maximum gain of ~1.25. This confirms that the bilayer NC stack works properly and can potentially enhance the switching rate of a transistor when used as the gate stack. Next, we fabricated MoS_2 FETs by transferring an exfoliated tri-layer MoS_2 film onto the bilayer gate stack and formed source/drain contacts by electron-beam lithography. Fig. 4(a) and (b) show schematics of the NC-MoS_2 FET with a bilayer gate stack and the reference MoS_2 FET with only HfO_2 as the gate dielectric. Fig. 4(c) compares the transfer characteristics of the reference and NC devices. The measurements were performed in vacuum to eliminate the hysteresis induced by physisorbed moisture on the MoS_2 channel. Both devices show small hysteresis (~17 mV). To guarantee that the device was in transient mode during the measurement and thus enters the NC regime, the point-to-point delay time during the gate voltage sweep was set to 100 μs. This was the minimum value allowed by the measurement setup and was sufficiently smaller than the gate RC delay time (>5 ms). The device has an on current of 5 μA μm^{-1} and maximum transconductance of 12 μS μm^{-1}, and the off current is as low as 1 pA μm^{-1}. The subthreshold characteristics of the device are of particular importance. In Fig. 3(b), the developed gate stack allows internal gain of up to 1.25 times. This internal gain can improve the subthreshold swing of the transistor and allows the 60 mV dec^{-1} limit to be overcome without changing the transport mechanism. As shown in Fig. 4(d), the reference device has SS_{min} = 67 mV dec^{-1} at a current level of ~10 pA μm^{-1} (Fig. 4(d)). The deviation of the SS from 60 mV dec^{-1} is attributed to trapped charges at the MoS_2/oxide interface, which lower the gate efficiency and thus increase the SS. The NC FET with the same MoS_2 channel length and thickness as well as the same MoS_2/oxide interface shows significantly improved SS with a minimum of 57 mV dec^{-1}, which is in agreement with the observed voltage amplification in Fig. 3(b). For the NC-MoS_2 FET, this allows transistor operation with $I_{off} < 10$ pA μm^{-1} and $I_{on}/I_{off} > 10^5$ with a ΔV_{gs} of 0.5 V compared with a required ΔV_{gs} of ~0.65 V to achieve the same performance in the reference MoS_2 FET. Because the channel/oxide interface can degrade the SS, the SS can be further reduced by developing an ultraclean MoS_2/oxide interface. Moreover, further optimization of the capacitance matching in the bilayer stack can improve the voltage amplification factor and thus further increase the gate efficiency.

It should be noted that NC technology is in its infancy and several aspects need to be experimentally investigated. In

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particular, for targeted applications in state-of-the-art high-performance CMOS technology, the switching performance of NC FETs and the effects of dielectric thickness scaling and the gate-leakage current at high gate switching speeds on the amplification capability of the NC bilayer stack need to be extensively investigated.

Conclusions

In summary, NC-MoS_2 FETs were fabricated using a CMOS compatible Al : HfO_2 ferroelectric thin film. ALD Al : HfO_2 films with different Al : Hf ratios were deposited on Si substrates and characterized by XPS, which showed excellent Al : Hf ratio control and dopant homogeneity in the host lattice. Gate voltage amplification up to 1.25 times was then demonstrated by incorporation of 10 nm 7.3% Al : HfO_2 in the dielectric stack of a MoS_2 FETs with 10 nm HfO_2 as a positive linear dielectric. The NC-MoS_2 FET showed a significant enhancement of the SS to 57 mV dec^{-1}, while the absence of hysteresis showed the effective stabilization of the NC by using the HfO_2/Al : HfO_2 bilayer.

Experimental

All the electrical measurements were performed under vacuum with a Keysight B1500A Semiconductor Device Analyzer with a mid-power SMUs with a sweep measurement resolution of 100 μs. Briefly, the MoS_2 devices were prepared by the commonly used pickup and dry transfer method. The MoS_2 was mechanically exfoliated to obtain isolated flakes of a few layers, from commercially available bulk MoS_2 crystals on precleaned (piranha solution, oxygen plasma, and solvent) substrates. A polydimethylsiloxane (PDMS) sheet was placed on a precleaned glass slide. A 6%-solution of polypropylene carbonate (PPC, Sigma-Aldrich) in chloroform was then spin coated on the glass/tape/PDMS stack. This transfer slide was loaded into the probe arm of the transfer setup and brought into contact with the desired flake at room temperature. The stage was heated to 90 °C and maintained at that temperature for 1 min. After cooling the stage, the transfer slide was then slowly disengaged. The picked-up flake was transferred to the target substrate and heated to 155 °C to release the polymer. The polymer was dissolved in chloroform and the structure was cleaned with solvent and annealed in an Ar atmosphere at 360 °C for 3 hours.

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Notes and references

1 Y. Yoon, K. Ganapathi and S. Salahuddin, *Nano Lett.*, 2011, **11**, 3768–3773.
2 W. Cao, J. Kang, D. Sarkar, W. Liu and K. Banerjee, *IEEE Trans. Electron Devices*, 2015, **62**, 3459–3469.
3 A. Nourbakhsh, A. Zubair, S. Huang, X. Ling, M. S. Dresselhaus, J. Kong, S. De Gendt and T. Palacios, 15-nm channel length MoS_2 FETs with single- and double-gate structures, in *2015 Symposium on VLSI Technology*, 2015, pp. T28–T29, DOI: 10.1109/VLSIT.2015.7223690.
4 R. T. P. L. S. S. P. R. W. T. L. Yang, 2015 73rd Annual Device Research Conference (DRC), pp. 237–238, DOI: 10.1109/DRC.2015.7175655.
5 R. H. Yan, A. Ourmazd and K. F. Lee, *IEEE Trans. Electron Devices*, 1992, **39**, 1704–1710.
6 X. L. Chen, Z. F. Wu, S. G. Xu, L. Wang, R. Huang, Y. Han, W. G. Ye, W. Xiong, T. Y. Han, G. Long, Y. Wang, Y. H. He, Y. Cai, P. Sheng and N. Wang, *Nat. Commun.*, 2015, **6**, 6088.
7 E. J. G. Santos and E. Kaxiras, *ACS Nano*, 2013, **7**, 10741–10746.
8 B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti and A. Kis, *Nat. Nanotechnol.*, 2011, **6**, 147–150.
9 A. Nourbakhsh, A. Zubair, R. N. Sajjad, A. K. G. Tavakkoli, W. Chen, S. Fang, X. Ling, J. Kong, M. S. Dresselhaus, E. Kaxiras, K. K. Berggren, D. Antoniadis and T. Palacios, *Nano Lett.*, 2016, **16**(12), 7798–7806.
10 R. N. Sajjad, W. Chern, J. L. Hoyt and D. A. Antoniadis, *IEEE Trans. Electron Devices*, 2016, **63**, 4380–4387.
11 S. Salahuddin and S. Dattat, *Nano Lett.*, 2008, **8**, 405–410.
12 A. I. Khan, K. Chatterjee, B. Wang, S. Drapcho, L. You, C. Serrao, S. R. Bakaul, R. Ramesh and S. Salahuddin, *Nat. Mater.*, 2015, **14**, 182–186.
13 S. Dasgupta, A. Rajashekhar, K. Majumdar, N. Agrawal, A. Razavieh, S. Trolier-Mckinstry and S. Datta, *IEEE J. Explor. Solid-State Computat. Devices Circuits*, 2015, **1**, 43–48.
14 A. I. Khan, K. Chatterjee, J. P. Duarte, Z. Y. Lu, A. Sachid, S. Khandelwal, R. Ramesh, C. M. Hu and S. Salahuddin, *IEEE Electron Device Lett.*, 2016, **37**, 111–114.
15 F. A. McGuire, Z. H. Cheng, K. Price and A. D. Franklin, *Appl. Phys. Lett.*, 2016, **109**, 093101.
16 A. Rusu, G. A. Salvatore, D. Jimenez and A. M. Ionescu, *2010 IEEE International, Electron Devices Meeting (IEDM)*, 2010, 16.3.1–16.3.4, DOI: 10.1109/iedm.2010.5703374.
17 J. Muller, T. S. Boscke, U. Schroder, S. Mueller, D. Brauhaus, U. Bottger, L. Frey and T. Mikolajick, *Nano Lett.*, 2012, **12**, 4318–4323.
18 M. Hoffmann, M. Pešić, K. Chatterjee, A. I. Khan, S. Salahuddin, S. Slesazeck, U. Schroeder and T. Mikolajick, *Adv. Funct. Mater.*, 2016, **26**, 8643–8649.
19 P. D. Lomenzo, P. Zhao, Q. Takmeel, S. Moghaddam, T. Nishida, M. Nelson, C. M. Fancher, E. D. Grimley, X. Sang, J. M. LeBeau and J. L. Jones, *J. Vac. Sci. Technol., B*, 2014, **32**, 03D123.

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20 S. Mueller, J. Mueller, A. Singh, S. Riedel, J. Sundqvist, U. Schroeder and T. Mikolajick, *Adv. Funct. Mater.*, 2012, **22**, 2412–2417.
21 A. I. Khan, D. Bhowmik, P. Yu, S. J. Kim, X. Q. Pan, R. Ramesh and S. Salahuddin, *Appl. Phys. Lett.*, 2011, **99**, 113501.
22 A. I. Khan, U. Radhakrishna, K. Chatterjee, S. Salahuddin and D. A. Antoniadis, *IEEE Trans. Electron Devices*, 2016, **63**, 4416–4422.
23 A. I. Khan, C. W. Yeung, C. M. Hu and S. Salahuddin, 2011 Ieee International Electron Devices Meeting (Iedm), 2011.

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