15-nm Channel Length MoS_2 FETs with Single- and Double-Gate structures

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Abstract: We demonstrate single- and double-gated (SG & DG) field effect transistors (FETs) with a record source-drain length ($L_{S/D}$) of 15 nm built on monolayer (t_{ch}~0.7 nm) and 4-layer (t_{ch}~3 nm) MoS_2 channels using monolayer graphene as the Source/Drain contacts. The best devices, corresponding to DG 4-layer MoS_2-FETs with $L_{S/D}$=15 nm, had an I_{on}/I_{off} in excess of 10^6 and a minimum subthreshold swing ($SS_{min.}$) of 90 mV/dec. at V_{DS}=0.5 V. At $L_{S/D}$=1 μm and V_{DS}=0.5 V, $SS_{min.}$=66 mV/dec., which is the best SS reported in MoS_2 FETs, indicating the high quality of the interface and the enhanced channel electrostatics.

Introduction: Atomically thin-films of layered semiconductors such as MoS_2 have great potential in device applications because of their ultra-thin body nature, large bandgap, thermal stability and compatibility with CMOS processes [1, 2]. MoS_2 FETs have an extremely low I_{off}, making them promising for low power applications [2]. Also, FETs built on a few layers of MoS_2 are effectively ultra-thin body FETs (UTB-FETs), which are immune to short channel effects (SCE) [3]. Also, the smaller dielectric constant (ε_s) of MoS_2 compared with Si (6.8~7.1 *vs* 11.9) can further suppress the SCE [4]. The minimum channel length required to maintain long channel behavior is on the order of 4 times the characteristic length ($L_{min}=4\lambda$), where $\lambda=\sqrt{(1/N).\sqrt{(\varepsilon_s.t_s.t_{ox}/\varepsilon_{ox})}}$ for a planar FET, ε_s/t_s and ε_{ox}/t_{ox} are the dielectric constant/thickness of the channel and oxide, respectively and N=1 for SG and N=2 for DG FETs. However, this formula assumes that the S/D electric field lines are mostly confined in the channel to minimize the impact from the surrounding environment. For this, the S/D electrodes that are in immediate contact with the channel need to be as thin as the channel. To meet this requirement, monolayer graphene (t~0.4 nm), was used as the S/D in this work.

Device Fabrication: The key steps for fabricating SG & DG MoS_2 FETs with graphene S/D contacts, as well as a schematic of the devices are shown in Fig. 1. Either CVD grown monolayer or a mechanically exfoliated 4-layer MoS_2 was transferred onto a [p^+ Si/native SiO_2] substrate coated with 10 nm of HfO_2 (EOT=3.3 nm) as the back gate (BG). Subsequently, monolayer graphene was transferred onto the MoS_2 layer. High resolution PMMA trenches ranging from 60 to 15 nm were patterned on the MoS_2/graphene stack by the cold development (−15 °C) of 25 nm thick PMMA films followed by selective etching of the graphene with a mild indirect pulsed O_2 plasma, opening narrow slits down to 15 nm in the conductive graphene layer, defining the S/D channel. This process, which is suitable for UTB-FETs, is comparable to the metal dry-etching process used to fabricate S/D and gate electrodes in advanced CMOS fabrication [5]. Details on the pulsed plasma etch process are reported in [6]. After dry removal of the PMMA by a forming gas anneal, 1 nm air-oxidized Al_2O_3 was deposited as a seed layer for subsequent ALD deposition of 10 nm HfO_2 and 50 nm of Ni gate electrode onto the channel to build the top gate (TG). Fig. 2 shows an AFM image of the graphene slits ranging from 10 to 20 nm before TG deposition.

Results and discussion: The sheet resistance characteristics of monolayer graphene after different numbers of O_2 plasma pulses are depicted in Fig. 3(a). After a sufficient number of pulses, graphene is eventually etched away, leaving a well-defined graphene slit, which defines the atomically-thin S/D contact. The etching of the graphene was well controlled with minimum impact on the underlying MoS_2 layer, as confirmed by Raman spectroscopy (Fig. 3(b)). The capacitance-voltage (C-V) characteristics depicted in Fig. 4 show that MoS_2 is a natural *n*-type semiconductor. Therefore, MoS_2-FETs operate in the accumulation-mode. Fig. 5 compares the transfer characteristics of long channel ($L_{S/D}$=1 μm) monolayer and 4-layer MoS_2 FETs. The monolayer FET had an I_{on}/I_{off} in excess of 10^7 and $SS_{min.}$=75 mV/dec, while the SG 4-layer FET had a smaller I_{on}/I_{off} and a larger SS_{min} (105 mV/dec) (Fig. 5(b)). This difference is attributed to the better channel electrostatic control in monolayer *vs* multilayer FETs. However, the performance can be significantly enhanced by adding a TG electrode, which improved the $SS_{min.}$ to 66 mV/dec and I_{on}/I_{off} to ~10^7 (Fig. 5(b)). Long and short channel DG monolayer MoS_2 FETs were not fabricated in this study as seeding ALD high-k dielectrics on monolayer MoS_2 drastically shifts the V_{th} and therefore I_{off}, while multilayer FETs are significantly less sensitive to the high-k deposition process. The transfer characteristics of 15, 30 and 60 nm SG monolayer MoS_2 FETs are compared in Fig. 6(a). The occurrence of SCE in the 15 and 30 nm FETs caused their I_{off} to drastically increase, which is in agreement with drain-induced barrier lowering (DIBL) (Fig. 6(b)) showing an upturn at $L_{S/D}$=30 nm. However, as expected, the SCE was stronger in the SG 4-layer FET, resulting in larger SS and I_{off} (see Figs 7). Nevertheless, the subthreshold characteristics of 4-layer MoS_2 could be significantly enhanced by integrating a TG, taking into account that favorably 4-layer MoS_2 has better potential for digital application due to its higher mobility resulting from its higher density of states and lower interface effects compared to monolayer MoS_2 [7]. Figs 8 & 9 show the device characteristics of a 4-layer MoS_2-FET in the DG configuration. The MoS_2 FET had I_{on}/I_{off}=~10^6, I_{on}=~50 μA/μm and $SS_{min.}$=90 mV/dec. at V_{DS}=0.5 V. For this device, $L_{min.}(=4\lambda)$ in its SG configuration was ~17 nm (>$L_{S/D}$=15 nm), while in DG $L_{min.}$=~11 nm, which is in agreement with the downshift of the upturn point in DIBL (Fig. 10) to $L_{S/D}$=15 nm with a relatively low maximum. The DIBL values indicate that the SCE was suppressed.

Conclusions: We have demonstrated MoS_2 UTB-FETs scaled-down to $L_{S/D}$=15 nm with monolayer graphene contacts. The best $L_{S/D}$=15 nm performance was achieved in a DG 4-layer MoS_2-FET with I_{on}/I_{off}=10^6 and $SS_{min.}$=90 mV/dec. at V_{DS}=0.5 V. This transistor has the shortest operating channel length of any MoS_2 transistor to date. The device performance indicates further scaling to sub $L_{S/D}$=10 nm is possible.

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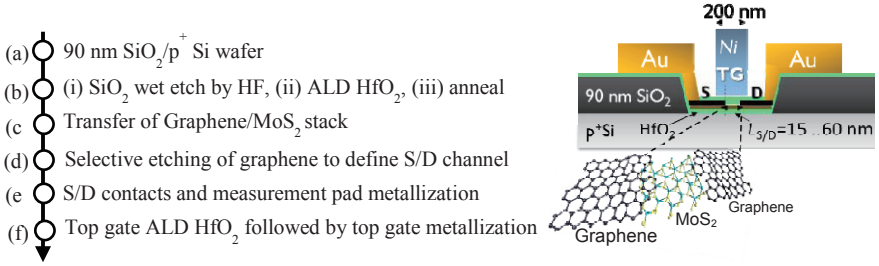


Fig. 1. Fabrication process flow and device schematic cross-section of the short channel SG & DG-MoS_2 FETs with graphene S/D contacts. Step (b) includes ALD-HfO_2 at 200 °C, followed by annealing in a forming gas at 400 °C. The SG-FETs fabrication process excludes step (f).

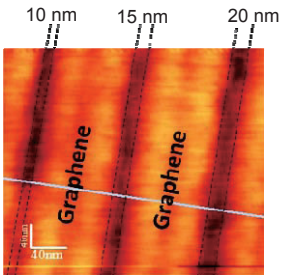


Fig. 2. AFM images showing 10, 15 and 20 nm graphene slits, after the PMMA was removed in an Ar/H_2 atmosphere at 360 °C.

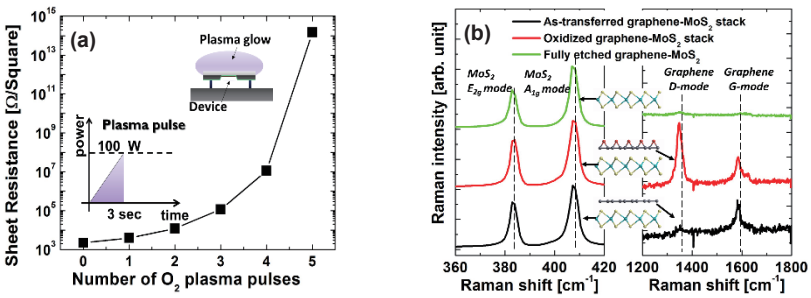


Fig. 3. (a) Graphene (oxide) sheet resistance *vs* number of O_2 pulses. The insets show schematics of a plasma pulse (power ramp from 0 to 100 W in 3 s) and the plasma setup with a device placed upside-down for indirect plasma exposure. (b) The evolution of Raman spectra of O_2 plasma-treated graphene-MoS_2 stack.

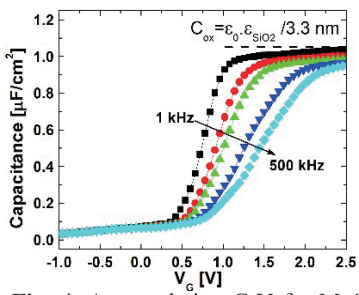


Fig. 4. Accumulation C-V for MoS_2 MOS capacitor with EOT=3.3 nm.

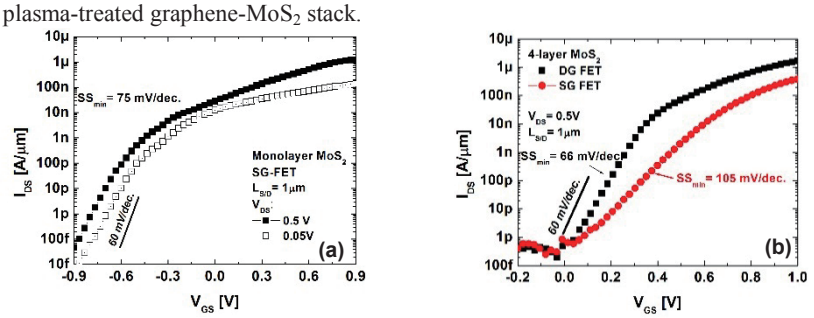
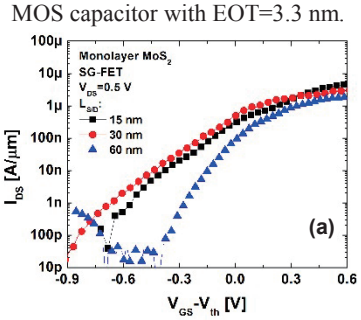


Fig. 5. Room temperature transfer characteristics of a 1 μm long channel (a) SG monolayer MoS_2 FET and (b) SG and DG 4-layer MoS_2 FETs.



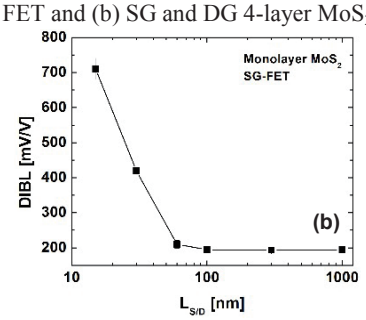


Fig. 6. (a) Transfer characteristics of 15, 30 and 60 nm SG monolayer MoS_2 FETs with graphene S/D contacts. (b) DIBL of monolayer SG MoS_2 FETs at various $L_{S/D}$ values. There is an upturn at $L_{S/D}$~30 nm and a DIBL saturation of ~200 mV/V.

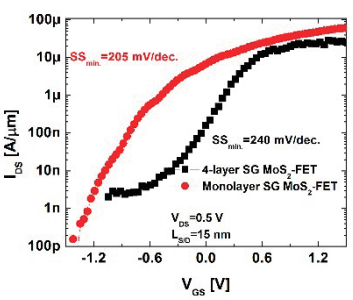


Fig. 7. Transfer characteristics of $L_{S/D}$=15 nm SG monolayer and 4-layer MoS_2-FETs. The stronger SCE in the 4-layer FET caused a larger I_{off} and increased SS_{min} compared with their respective values in the monolayer FETs.

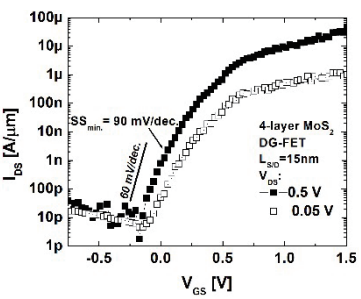


Fig. 8. I_{DS} *vs* V_{GS} for a $L_{S/D}$=15 nm 4-layer DG MoS_2 FET with record performance values including $SS_{min.}$=90 mV/dec. and I_{off} <10 pA/μm.

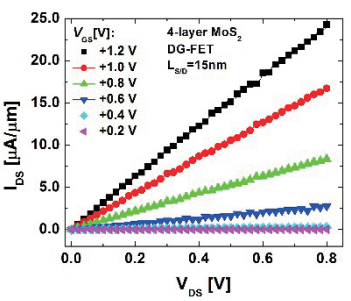


Fig. 9. I_{DS} *vs* V_{DS} for the MoS_2-FET in Fig. 8 for various V_{GS} values.

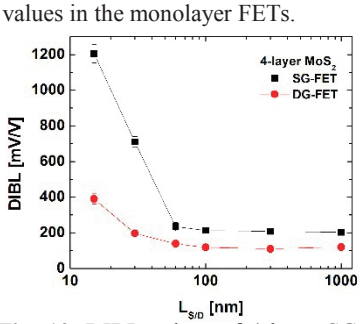


Fig. 10. DIBL values of 4-layer SG & DG FETs. The DG has a downshifted upward turning point compared with the SG FET and its maximum shows a three-fold decrease.