

CMOS electronics probe inside a cellular network

— Invited review paper —

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Abstract—The parallelization of intracellular recording can greatly benefit the study of complex neuronal networks, but it has proven difficult to achieve. To meet this challenge, we have been developing large-scale arrays of intracellular vertical nanoscale electrodes operated by underlying CMOS integrated circuits. The development has been fruitful, and our first-generation CMOS nanoelectrode array hit a milestone by intracellularly recording from up to 235 networked cardiomyocytes in parallel. We reported this first-generation system and its unprecedented parallelism in intracellular recording in *Nature Nanotechnology* 12, 460 (2017). The present paper is a review of this work with a special focus on the development of its CMOS integrated circuit.

Keywords—*electrophysiology; neuroscience; cardiology; nano-bio interface; nanotechnology; nanoelectrode array; CMOS integrated circuit; intracellular recording*

I. INTRODUCTION — CMOS NANO-ELECTRODE ARRAY

Device scaling into higher densities is synonymous with CMOS fabrication technology, and has been a basis of today's computing and information technology. In more recent years, this scalability is being increasingly attempted for applications in the life sciences, especially by constructing large-scale integrated device arrays that can detect aqueous ions, biological molecules, and cellular potentials with high parallelism. A case in point is an array of millions of ion-sensitive field-effect transistors implemented on a CMOS chip to perform all-electrical DNA sequencing [1]. Another example, in direct relevance to the present paper, is the CMOS microelectrode array (MEA) for electrophysiology [2]–[9]. The CMOS MEA can contain tens of thousands of microscale planar electrodes and thousands of electronics channels to record action potentials from a large number of electroactive cells such as neurons. This parallelism of the CMOS MEA makes a world of difference from the patch clamp electrode, which is difficult to parallelize due to its bulky setup.

In recording quality, the patch clamp electrode far transcends the CMOS MEA. Since the MEA is limited to extracellular recording, it has a much poorer signal-to-noise ratio and can measure only action potentials. In contrast, the patch clamp electrode [10] reaches a far higher sensitivity through intracellular recording and measures the full suite of membrane potentials that include not only action potentials

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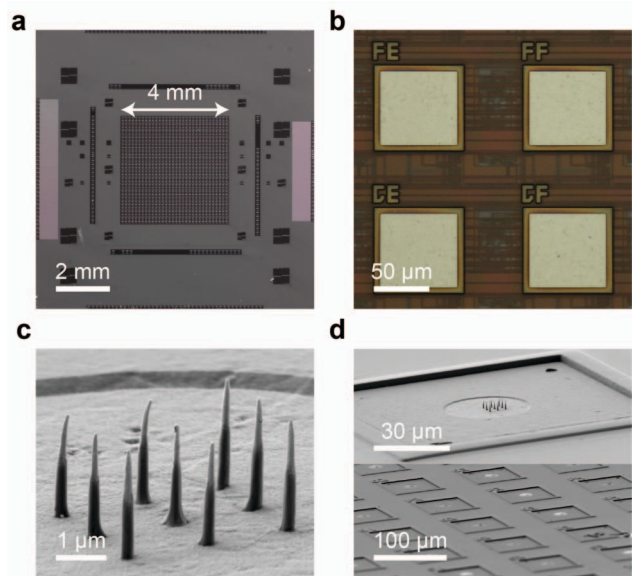


Fig. 1. CNEA. (a) CMOS IC (10.5 mm × 10.5 mm) fabricated in 0.35-μm technology. The 32 × 32 pixel array occupies 4.0 mm × 4.0 mm in the center region. (b) 4 pixel pads in the 32 × 32 pixel array on the IC surface. Each pad occupies 80 μm × 80 μm. The center-to-center pitch between two adjacent pads is 126 μm. Under each pad lie an amplifier, a stimulator, and a memory. (c, d) SEM images of post-fabricated 9 vertical nanoelectrodes per pad. Each nanoelectrode consists of a metal (Au or Pt) coating on a vertical SiO₂ core and a SiO₂ passivation layer that covers the metal coating except its tip portion. The metal coating makes a contact with cell cytosol at its tip and connects to the underlying pixel pad. The passivation layer is to form tight seal to the cell membrane. Each nanoelectrode has a tip diameter of ~100 nm and a height of 3 μm. Electrode-to-electrode pitch is 2 μm.

but also much smaller, yet telltale, postsynaptic potentials [11]. The patch clamp electrode has thus been instrumental in studying the fundamental cellular processes governing the electrical activities of neurons and other excitable cells.

The combination of parallelism (as in the CMOS MEA) and the high-quality intracellular recording (as in the patch clamp electrode) will take electrophysiology to a new horizon. For example, the parallelization of intracellular recording will significantly benefit the study and engineering of the complex neuronal networks by helping draw their functional connectivity map in detail. For another example, parallel intracellular recording will enhance the throughput of electrophysiological screening of drugs for neuronal or cardiac diseases. While developing a tool that possesses both traits—parallel and intracellular—has been a significant challenge, nanometer scale electrodes are offering new lines of attack.

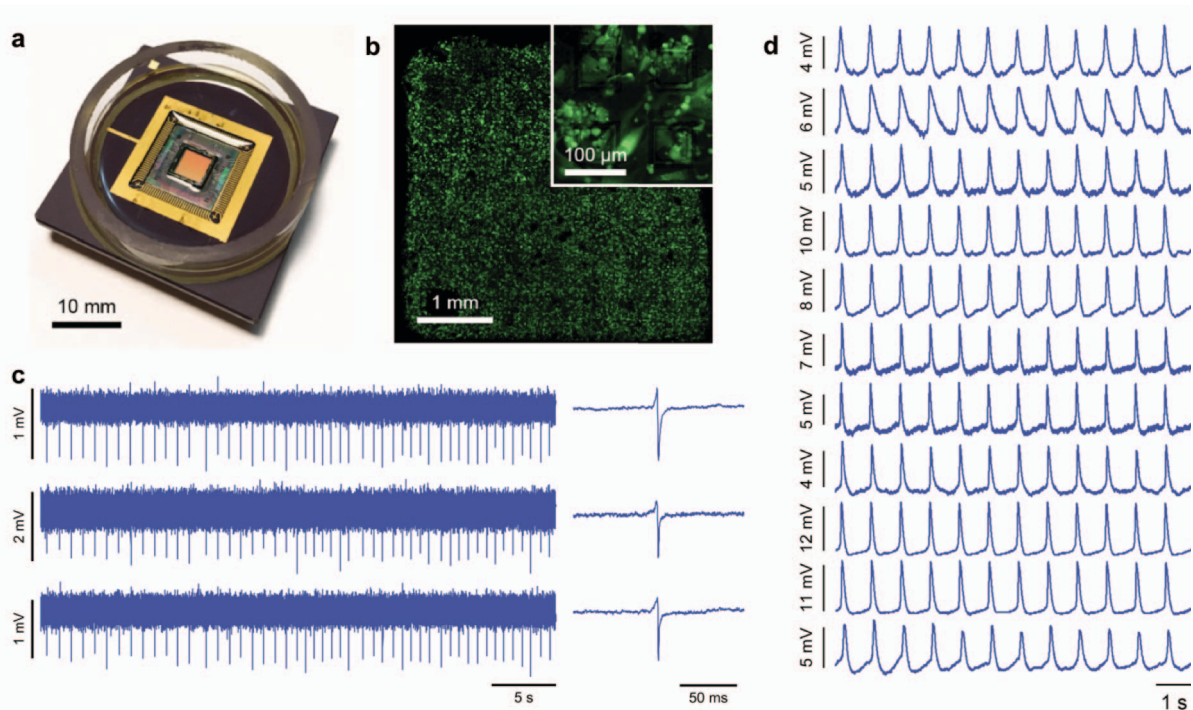


Fig. 2. (a) Packaged CNEA. (b) Fluorescence image of cardiomyocytes cultured on the CNEA. (c) Extracellular recordings from 3 example pixels before electroporation (left); averaged extracellular action potentials (right). (d) Intracellular recordings after electroporation from 11 example pixels. Parallel intracellular recording from up to 235 cardiomyocytes was achieved. Comparison to (c) shows that intracellular recording has a much higher signal-to-noise ratio.

First off, three-dimensionally structured nanoelectrodes [12]–[23], such as vertically standing nanoelectrodes [12]–[14], [21]–[23], have been shown to perform intracellular recording of mammalian cardiomyocytes [12], [14], [21] and neurons [13], [22], [23], making direct contacts with their cytosols. Second, since the size of these nanoelectrodes is comfortably within the reach of standard top-down fabrication [13], not only can the nanoelectrodes be constructed into massive scale arrays for parallelism, but they can be integrated with CMOS electronics to facilitate the operation of the massively parallel array and the handling of the large amount of data acquired.

Building on this vision, we have been developing nanoelectrode arrays on CMOS integrated circuits (ICs). We reported our first-generation CMOS nanoelectrode array (CNEA) (Fig. 1) in the journal *Nature Nanotechnology* in 2017 [21]. Its underlying CMOS IC contains $32 \times 32 = 1,024$ pixels, where each pixel consists of an amplifier (to record), a stimulator (to excite), and a 10-bit memory. In each pixel, the amplifier and stimulator are both connected to a metallic pad right above on the IC surface. 9 vertical nanoelectrodes are post fabricated in the center region of each pixel pad using the standard top-down process (Figs. 1c & 1d), and are addressed together electrically. The CNEA recorded intracellularly from up to 235 networked cardiomyocytes in parallel (Fig. 2d), where these cells were cultured *in vitro* on the CNEA surface (Figs. 2a & 2b). This network-level intracellular recording was then used to study the influence of drugs on the cardiomyocyte network behavior with sub-threshold sensitivity. In sum, by combining intracellular nanoelectrodes with the scalability of CMOS technology, our first generation CNEA achieved unprecedented parallelism in intracellular recording.

The role of the on-site CMOS electronics here is decisive. First, the pixel nanoelectrodes, modeled [24] as a nonlinear Faradaic resistance R_a in parallel with a double layer capacitance C_a (~ 1 pF) (Fig. 3a), have a very high impedance due to their small surface area. For example, in the capacitive mode, intracellular signals are coupled to the nanoelectrodes via C_a , whose impedance is $30 \text{ M}\Omega \sim 160 \text{ G}\Omega$ in the electrophysiological signal bandwidth (1 Hz \sim 5 kHz). So the pixel nanoelectrodes pass only a small current when measuring an electrophysiological event. With an off-chip amplifier, this already small current would leak profusely through the parasitic capacitance of the long signal path before amplification [13]. In contrast, the *in situ* pixel amplifier right below the pixel nanoelectrodes greatly shortens the signal path and reduces the parasitic capacitance (C_p , Fig. 3a), mitigating attenuation substantially. Second, it is practically impossible to wire nanoelectrodes of every pixel in such a large-scale array out to an off-chip interface [2]. On-site multiplexing with the underlying IC aptly addresses this issue, significantly reducing the total number of wirings. Third, whereas using global control signals from off-chip electronics shared by all pixels results in limited functionality and controllability, the *in situ* programmable memory at each pixel allows for far more versatile, real-time control of individual pixels.

The present paper is not a new contribution but an invited review of the first generation CNEA. Its original report [21] focused on the concept and implementation of the overall system and electrophysiology experiments demonstrating large-scale intracellular recordings from hundreds of cells. The present review paper will focus on the development of the CMOS IC, which plays a critical role in scaling the nanoelectrodes into a large array with intracellular access.

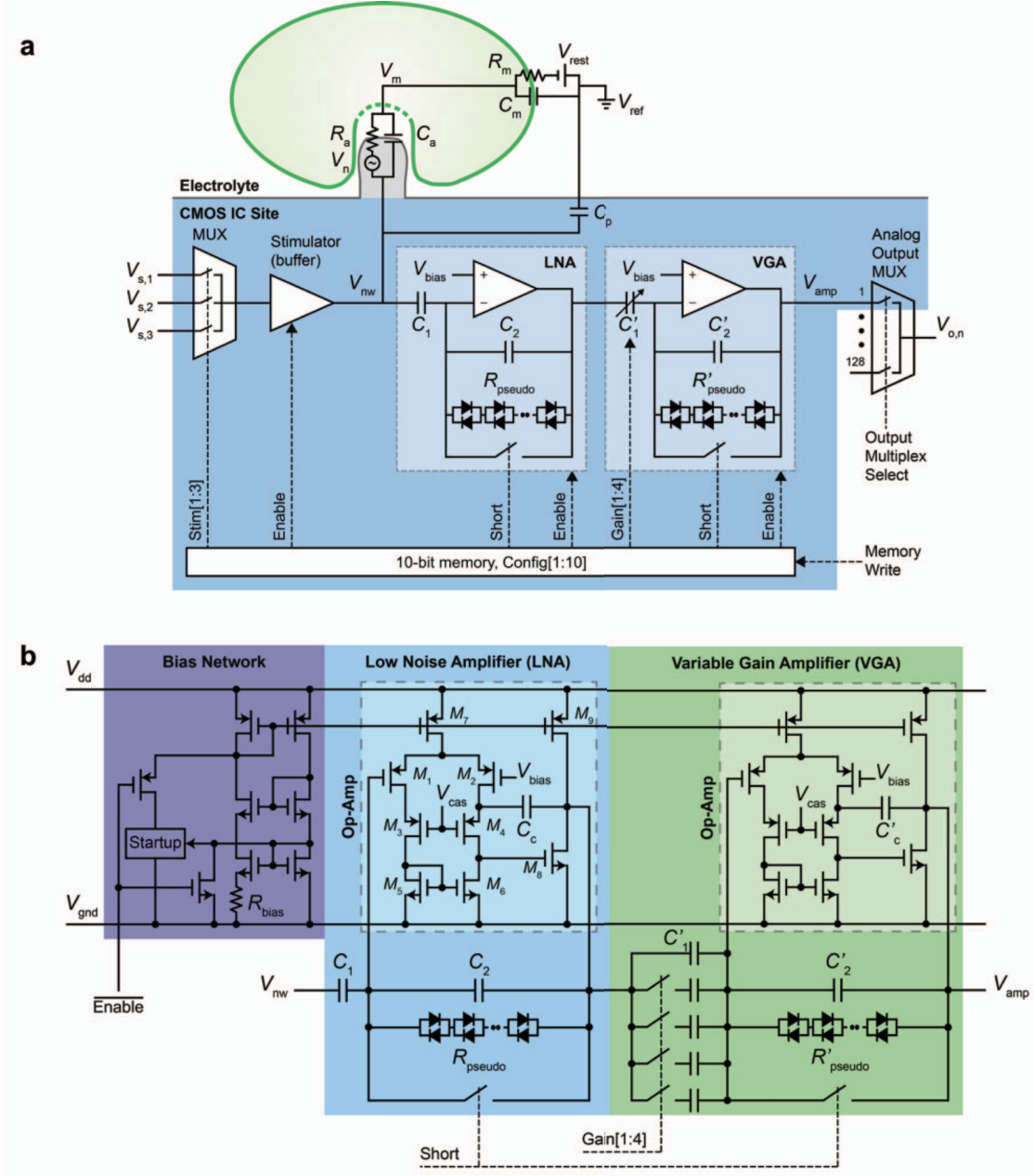


Fig. 3. (a) Individual pixel contains an amplifier (LNA + VGA), a stimulator, and a memory. The cell coupled with pixel nanoelectrodes is modeled using V_m , R_m , and C_m as membrane potential, resistance, and capacitance, and V_{rest} as resting potential. (b) Transistor-level schematic of the pixel amplifier.

II. DEVELOPMENT OF THE CMOS IC

A. Pixel architecture

Figure 3a is the architecture of the integrated pixel circuit consisting of an amplifier, a stimulator, and a 10-bit memory (Config[1:10]). The memory enables or disables the amplifier and stimulator, and controls their characteristics such as gain values and cutoff frequencies. The stimulator (voltage buffer) can apply a voltage signal with an amplitude of up to 4 V to the nanoelectrodes and is used to excite cells or to execute electroporation. The stimulator is accompanied by a 3-bit multiplexer (Stim[1:3]), which chooses any one of 3 different excitation signals routed to all pixels for the stimulator. The

amplifier is by far the most non-trivial component to design, for it is to process small electrophysiological signals registered at the high-impedance pixel nanoelectrodes. It must achieve an optimal set of gain, noise, bandwidth, and input impedance within the constraints of area (to achieve a dense array) and power (to minimize heat dissipation that can impair cells).

B. Pixel amplifier – transfer characteristics

The pixel amplifier consists of a low noise amplifier (LNA) followed by a variable gain amplifier (VGA) (Fig. 3a). The front-end LNA is the most critical building block in setting the sensitivity of the overall amplifier. The VGA provides an additional gain that can be tuned, and dominantly determines the linearity of the overall amplifier.

The LNA is an op-amp (Fig. 3a) nested in a negative feedback loop consisting of capacitors C_1 and C_2 and pseudo-resistor R_{pseudo} . As the capacitor C_1 at the LNA input blocks DC currents to and from the pixel nanoelectrodes, during the recording mode, the nanoelectrodes operate in the capacitive mode instead of the Faradaic mode. The closed-loop topology of the LNA creates bandpass characteristics, rejecting slow drift of the nanoelectrode voltage as well as the noise outside the signal frequency range. The op-amp of the LNA has a 2-stage scheme with internal frequency compensation (Fig. 3b). The 1st stage is fully differential with 3 pairs of transistors (M_1+M_2 ; M_3+M_4 ; and M_5+M_6) in the signal path with M_1 and M_2 being the input transistors. The 2nd stage has a single-ended output at the shared drain node of transistors M_8 and M_9 . The open-loop gain of the LNA's op-amp is $\sim 4,000$. This is large enough to ensure that the gain of the LNA, which is the closed-loop gain of the op-amp, is C_1/C_2 in the passband. The VGA adopts the same topology and bandpass character as the LNA, but with generally different sizing of devices (Fig. 3b). The VGA gain in the passband is hence C_1'/C_2' , which can be varied with the use of a tunable C_1' consisting of 5 parallel capacitors with 4 of them accompanied by switches, which are controlled by the pixel memory (4 bits, Gain [1:4]). The passband gain of the overall amplifier is thus

$$G \equiv \frac{V_{\text{amp}}}{V_{\text{nw}}} = \frac{C_1}{C_2} \cdot \frac{C_1'}{C_2'} \quad (1)$$

While both the LNA and VGA have bandpass characters, our design sets the low and high cutoff frequencies, f_1 and f_2 , of the overall amplifier by the bandpass characteristics of the LNA. We aim at $f_1 \sim 1$ Hz and $f_2 \sim 5$ KHz to reject noise outside the bandwidth of electrophysiological signals [11]. The gain-bandwidth product of the open-loop op-amp in the LNA is g_{m1}/C_c , where g_{m1} is the transconductance of the input transistor M_1 (and M_2) and C_c is the Miller capacitor to set the minimum phase margin at 60° . Since the gain-bandwidth product remains the same for the LNA, which is the op-amp in the closed loop, the LNA's bandwidth is given by g_{m1}/C_c divided by the LNA gain C_1/C_2 . Since this bandwidth is $f_2 - f_1 \cong f_2$ (as $f_2 \gg f_1$), we obtain

$$f_2 \cong \frac{g_{m1}}{C_c} \cdot \frac{C_2}{C_1} \quad (2)$$

Hence setting f_2 at 5 kHz requires the optimization of both size and bias current of relevant capacitors and transistors. To obtain $f_1 \sim 1$ Hz where

$$f_1 \cong \frac{1}{2\pi R_{\text{pseudo}} C_2}, \quad (3)$$

R_{pseudo} should be on the order of $T\Omega$, as C_2 is set at ~ 10 fF to optimize gain and noise. It is practically impossible to obtain such a large resistance with standard resistive materials in CMOS technology, so we use anti-parallel pn -junction diode pairs biased at zero DC current as R_{pseudo} (Fig. 3). The anti-parallel connection makes the diode response symmetric for positive and negative signals. Furthermore, to reduce nonlinearity of the resistor, multiple pairs of anti-parallel diodes are connected in series; this reduces voltage drop on each pair for a given signal, lessening nonlinearity. The time constant associated with $f_1 \sim 1$ Hz would slow down the

settling of the amplifier when it is turned on. We circumvent this by adding a switch controlled by the pixel memory (1 bit) to the negative feedback path of the LNA and by making the same arrangement for the VGA too (Fig. 3); these switches are turned on momentarily when the amplifier is activated.

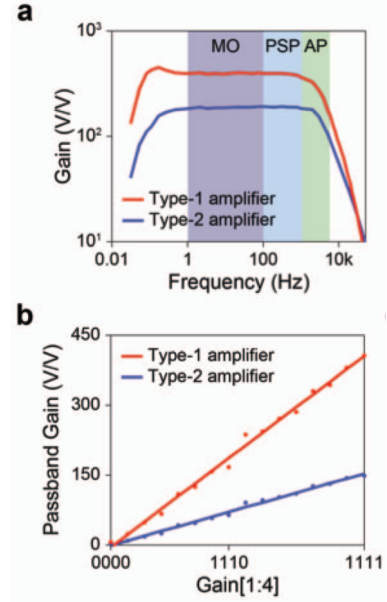


Fig. 4. (a) Measured transfer function ($V_{\text{amp}}/V_{\text{nw}}$) of a type-1 and a type-2 amplifier. Typical bandwidths of membrane oscillations (MO), postsynaptic potentials (PSP), and action potentials (AP) are shown. (b) Passband gain G ($V_{\text{amp}}/V_{\text{nw}}$ at 100 Hz) vs. VGA code for another type-1 & type-2 amplifiers.

In the top half of the array, each LNA's pseudo-resistor is a series of 10 pairs of small anti-parallel diodes, whereas that in the bottom half of the array is a series of 3 pairs of large anti-parallel diodes. The former gives a higher linearity, a larger R_{pseudo} , and a smaller pn junction parasitic capacitance. The VGA pseudo-resistor is a series of 10 pairs of small anti-parallel diodes all across the array, as linearity is of greatest importance in this second stage amplification. Hence the top and bottom halves of the array have two differing types of pixel amplifiers, referred to as type-1 and type-2 amplifiers. This arrangement is to examine the design trade-offs among various traits of the pseudo-resistor, as such pn -junction based ultra large resistance will remain essential for future generations of the CNEA. Figure 4a shows the measured transfer function at maximum gain (Gain[1:4] = 1111) for a type-1 and a type-2 amplifier. The type-1 amplifier has a smaller f_1 than the type-2 amplifier (0.05 Hz vs. 0.1 Hz) primarily because the LNA of the former uses a larger R_{pseudo} . And the type-1 amplifier has a larger gain, for the pseudo-resistor of its LNA has a smaller parasitic capacitance to add to C_2 . Figure 4b shows the passband gain G measured at 100 Hz as a function of the VGA code, Gain[1:4], from another set of type-1 and type-2 amplifiers. Again, G is larger for the type-1 amplifier. Also in either amplifier type, G linearly increases with the VGA code. As we measure the passband gain G of pixel amplifiers across the array, its variability remains consistent with process variations of the pseudo-resistor's parasitic pn junction capacitance.

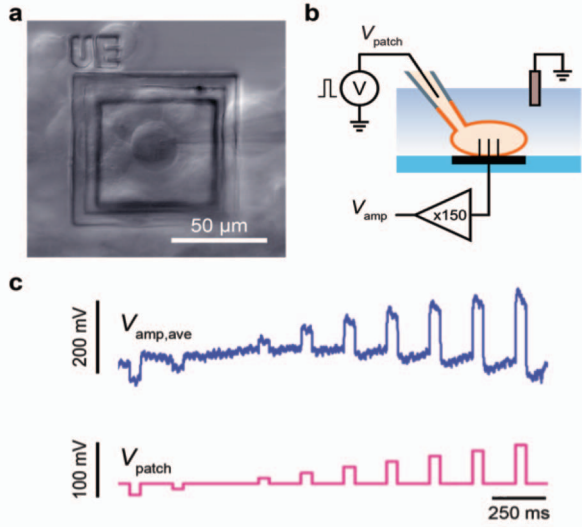


Fig. 5. (a) HEK293 cell on a pixel pad. (b,c) The pipette in voltage clamp mode applies signals and resulting membrane potentials are recorded by the CNEA pixel. $V_{amp,ave}$ is the average of 50 repeated V_{amp} data.

While Fig. 4 showed the signal transfer from the amplifier input (V_{nw}) to the output (V_{amp}), Fig. 5 shows an experiment to examine the signal transfer through the electrode-amplifier chain (V_m to V_{amp}). This experiment utilizes an *in vitro* cultured human embryonic kidney (HEK) 293 cell intracellularly coupled with the nanoelectrodes on a pixel pad with a type-2 amplifier underneath (Fig. 5a). The cell is also patched by a pipette (Fig. 5b). Signal V_{patch} applied by the patch pipette (Fig. 5c, bottom) results in membrane potential V_m , which should be approximately equal to V_{patch} due to the low impedance of the pipette in the voltage clamp mode. $V_m \sim V_{patch}$ is then recorded by the nanoelectrode-amplifier chain to yield V_{amp} (Fig. 5c, top; averaged over 50 repeats). The largest applied pulse of $V_{patch} \sim V_m \sim 70$ mV results in a recorded V_{amp} of ~ 200 mV. Dividing this by the amplifier gain $G = 152$ V/V implies that a voltage pulse of $V_{nw} \sim 1.3$ mV appears at the amplifier input. From this, we make two observations. First, this V_{nw} peaks amply above the amplifier's input-referred noise ~ 250 μ Vrms (see Sec. II-C). Second, the attenuation factor $\alpha = V_{nw}/V_m \sim 0.02$ V/V is 6 times improved as compared to the stand-alone nanoelectrodes in the same capacitive mode [13], attesting to the benefits of *in situ* amplification. Finally, the conservation of the waveform seen in Fig. 5c verifies intracellular access and a linear, flat-band transfer function from the cell cytosol to amplifier output. The slow oscillation of the amplifier output (Fig. 5c, top) is due to the low frequency high-pass pole of the bandpass filter configuration of the pixel amplifier.

C. Pixel amplifier – noise characteristics

As the signal flows through the electrode-amplifier chain, it is contaminated by noise. First, the Johnson noise V_n (Fig. 3) from the nanoelectrode resistor R_a stores an *rms* voltage noise $[kT/(C_a+C_p+C_1)]^{1/2}$ onto the total capacitance $C_a+C_p+C_1$ at the amplifier input. This sets the initial signal-to-noise ratio. To this does the LNA add noise (we will ignore the less critical noise contamination through the VGA). Due to the low-frequency spectral contents of the electrophysiological signals,

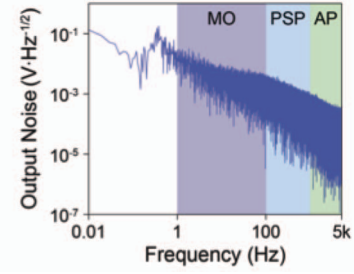


Fig. 6. Output voltage noise PSD of a type-2 amplifier.

we will have to consider not only the thermal noise but also the $1/f$ noise. The input-referred noise power spectral densities (PSDs) of the LNA due to the $1/f$ and thermal noise are

$$\frac{V_{n,f}^2}{\Delta f} \propto \frac{1}{W_1 L_1 f} \cdot \left[1 + \beta \left(\frac{L_1}{L_5} \right)^2 \right] \times \frac{(C_{M1} + C_{eq} + C_2)^2}{C_1^2} \quad (4)$$

$$\frac{V_{n,th}^2}{\Delta f} \propto \frac{kT}{g_{m1}} \cdot \left[1 + \gamma \left(\frac{W_5 L_1}{L_5 W_1} \right)^{1/2} \right] \times \frac{(C_{M1} + C_{eq} + C_2)^2}{C_1^2} \quad (5)$$

where C_{M1} is the gate capacitance of transistor M_1 , $C_{eq} \equiv C_1(C_a+C_p)/(C_1+C_a+C_p)$, L_1 and W_1 are the channel length and width of transistor M_1 (and M_2), L_5 and W_5 are the channel length and width of transistor M_5 (and M_6), and β and γ are empirical parameters on the order of 1 variable with process. Analysis of these equations show that the LNA noise tends to be smaller when transistors in the signal path are larger and sink more current, while this optimization should be done with the constraints of the pixel area, power budget, and gain-bandwidth product. Figure 6 shows the PSD of the output voltage noise measured with a type-2 amplifier at its maximum gain. The corresponding input-referred noise at the V_{nw} node integrated over the amplifier bandwidth is ca. 250 μ Vrms. This value is largely consistent through the array.

In addition to the devices' thermal and $1/f$ noise, we should minimize the impact of the fluctuations of the chip ground V_{gnd} on the output of the amplifier. To this end, we add cascode transistors M_3 and M_4 to the op-amp of the LNA (and the same measure is taken for the VGA) (Fig. 3b). This improves the V_{gnd} -associated power supply rejection ration (PSRR) to 46 dB for the pixel amplifier. While the cascoding introduces another bias V_{cas} , this does not draw current and thus is far quieter than V_{gnd} . The V_{dd} -associated PSRR is high (44 dB) even before the cascoding. The tail bias currents for the LNA and VGA are set by an auxiliary bias network shown on Fig. 3b, left. This network produces bias currents independent of temperature fluctuations to the first order. As the network has a metastable state at zero current, to ensure that it bootstraps into the state where it generates the tail bias currents for the amplifier, we implement a startup circuit that injects current into the network when it is turned on.

After considering all performance aspects discussed in this and foregoing subsection, the pixel amplifier design reached a balance among the amplifier parameters with a pixel area of $126 \mu\text{m} \times 126 \mu\text{m}$ and a maximum designed amplifier power consumption of $12 \mu\text{W}$ or a maximum power dissipation density of ~ 76 mW/cm² across the array, which is in good agreement with the maximum power dissipation density of ~ 62 mW/cm² measured with all amplifiers on.

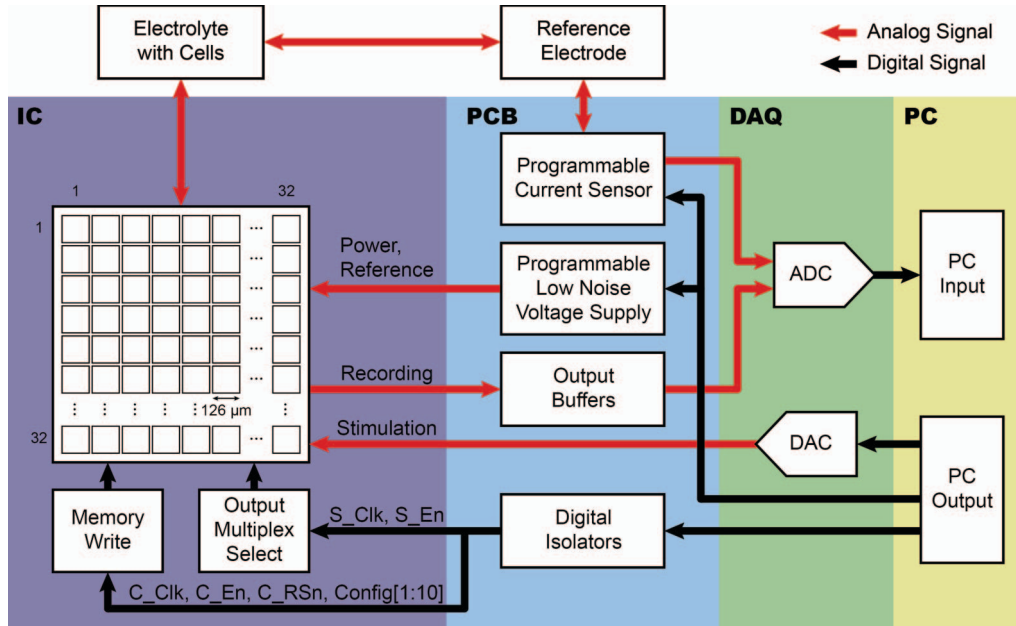


Fig. 7. Gross operation of the CNEA.

D. Gross operation of the CNEA

Figure 7 illustrates the setup to operate the CNEA. The CMOS IC and a printed circuit board (PCB) are programmed and read through a National Instruments PXIe-6358 data acquisition (DAQ) card and interfaced to the PC via a real-time custom Labview software. A digital block ‘memory write’ integrated outside the array but on the CMOS IC, receives configuration data bits (Config[1:10]) as well as configuration clock (500 kHz), enable, and reset (C_Clk, C_En, and C_RS_n) signals from the DAQ card. It then programs the 1,024 pixel memories sequentially at half the configuration clock rate; the programming of the entire array thus takes ~ 4.1 ms.

The 1,024 amplifier outputs are divided into 8 subgroups, with each containing 128 outputs from 4 rows of the array. The 128 outputs in each subgroup feed a 128:1 analog output multiplexer of its own (Fig. 3). This multiplexer continuously repeats, sampling the 128 outputs sequentially with a 1.248 MHz clock. Each amplifier output is then sampled at an effective rate of 9.75 kHz with no aliasing up to 4.875 kHz—chosen close to f_2 , the high cutoff of the amplifier. The 128 signals so sampled share the same data line. As a whole, 8 analog output data stream from the array, which are routed to 8 analog-to-digital converters of the DAQ card. For this multiplexing operation, the DAQ card produces the 1.248 MHz sample clock and sample enable signal (S_Clk and S_En), which are fanned out to the 8 analog output multiplexers by an integrated digital block, ‘output multiplex select’.

The biasing of the IC is facilitated by digitally programmable low-noise voltage regulators on the PCB. They provide the IC with a power supply, $V_{dd} = 5$ V, and amplifier input biases (V_{bias} in Fig. 3), with reference to chip ground, V_{gnd} . The chip ground is programmable from -5.0 V to $+5.0$ V with 1-mV accuracy with respect to the potential V_{ref} of the Ag/AgCl reference electrode in solution, which we set at earth ground; the amplifier input biases are programmable with

0.5 mV accuracy. This biasing scheme allows pixel stimulators to produce both positive and negative voltages with respect to V_{ref} . In addition to the voltage regulators, the PCB contains an inline current sensing circuit to measure the positive and negative current through the reference electrode from ~ 1 pA to 1 μ A.

III. LOOKING AHEAD

Our first generation CNEA has demonstrated highly parallel intracellular recordings from hundreds of *in vitro* cultured cardiomyocytes that form a network. This marks a first step towards high-fidelity investigations of complex electrogenic cellular networks. A next step will be to demonstrate the parallel intracellular recordings from a large number of *in vitro* cultured neurons. To do this meaningfully, the CNEA must be also improved, expanding the number of pixels and decreasing the pixel-to-pixel pitch to the same order as a single neuron. To accomplish this, new circuit techniques could be used to decrease the size of the pixel circuit: many ideas developed by CMOS MEAs [2]–[9] (which implement tens of thousands of electrodes) such as switch matrices or single transistor pixel amplifiers might be adapted. These techniques may need to be modified, however, to preserve the waveform shape, which is not important for extracellular recording. Smaller technology nodes could also help decrease transistor size and traces while providing additional metal layers for routing. Our current technology choice of 0.35 μ m hinged on the ability to apply ~ 4 V stimulations; but our experiments found that ~ 2.4 V signals were sufficient for electroporation, allowing 2.5 V technology nodes to be used. Further study of the cell-to-electrode interface could also offer additional techniques for intracellularly probing neurons. In contrast to our use of electroporation to gain intracellular access, a recent report showed high-fidelity recordings from neurons without the need for electroporation by using high aspect ratio nanoelectrodes [22] while a different study used a strong optical pulse to gain intracellular access [23]. Adopting

a similar technique or coupling it with a weaker electroporation may enable an effective intracellular interface. Overall, by coupling improvements in the cell-electrode interface and of the CMOS IC, simultaneous, long-term, multisite, intracellular recording and stimulation from a large number of neurons across a network may be achievable, opening up new fundamental studies in neuroscience. This is the direction that we have already taken.

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